IBM Field Engineering

Instruction - Reference

1414 Input-Output Synchronizer

Models 1, 2 and 7

IBM

Instruction–Reference

IBM 1414 Input-Output Synchronizer

Models 1, 2 and 7

Preface

This manual describes IBM 1414 Input-Output Synchronizer (Models 1, 2, and 7) operation with the following IBM Data Processing Systems: 1410, 7010, and 7044. To show the relation of the Model 1414, Model 1, 2, or 7 to other units in the system, brief descriptions of processing unit and channel actions that occur in the execution of magnetic tape operations are included. Detailed information on the processing unit in the IBM 1410 System is included in the *IBM Customer Engineering Manual of Instruction, 1411 Processing Unit Instructions and Special Features,* Form 223-2698, and in the *IBM Customer Engineering Instruction-Reference manual, 1410 System Fundamentals,* Form 223-2589. Complete information on data channels and processing unit operations in the IBM 7040 and 7044 Systems is included in the *IBM Customer Engineering Instruction-Reference manual, 7904 Data Channel, Preliminary Edition,* Form R23-2595-1, and in the *IBM Customer Engineering Manual of Instruction, 7106/7107 Central Processor, Preliminary Edition,* Form R23-2574. The *IBM Customer Engineering Instruction-Reference manuals, 7010 Data Processing System, Volumes 1 and 2, Preliminary Editions,* Forms R23-2364 and R23-2636, contain information on the processing unit in the 7010 System.

Included in this manual are second level diagrams of circuits for the IBM 1414, Models 1 and 2, explanations of the CE panel, and several checking procedures.

This manual obsoletes Form R23-2554-1.

MINOR REVISION AUGUST 1965

This manual, Form 223-2554-1, is a minor revision of the previous edition but does not obsolete Form 223-2554. The information presented herein has been corrected and brought up to the latest engineering level. Included is EC 281293, mandatory for 1414's connected to 7040/7044 systems.

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The IBM 1414 (Models 1, 2, and 7) Input-Output Synchronizer controls magnetic tape units operation with the IBM 1410, 7010, 7040, and 7044 Data Processing Systems. Because other models of the 1414 Input-Output (I-O) Synchronizer perform different functions, Models 1, 2, and 7 are called tape synchronizers.

Channels E and F on the 1410 System and channels E, F, G, and H on the 7010 System can accommodate one 1414 tape synchronizer per channel. On the 7040 and 7044 Systems, one 1414 tape synchronizer can be attached to data channels A, B, C, D, and E.

Each 1414 tape synchronizer includes a tape adapter unit and a control section.

The tape adapter unit:

1. Controls tape movement on the selected tape unit.
2. Supplies signals that the tape unit requires to write characters on magnetic tape.
3. Checks all characters written on magnetic tape.

The control section:

1. Provides for off-line testing of the tape synchronizer and tape units.
2. Processes all signals between the processing unit (1410/7010) or data channel (7040/7044) and the 1414 tape synchronizer.

Corresponding circuits in each tape synchronizer model function to accomplish the same purpose; data flow paths in the 1414 Models 1, 2, and 7 are identical. Only timings differ to perform specific functions in various tape unit models. Figure 1 lists the tape units that can be attached to each 1414 tape synchronizer model. Characteristics of magnetic tape units that 1414 tape synchronizers control are listed in Figure 2.

Tape Synchronizer Model	Tape Units
1414-1	729 II and 729 IV
1414-1 With Intermix Feature	729 II, 729 IV, and 7330
1414-1 With 800 cpi Feature	729 II, 729 IV and 729 V
1414-1 With Intermix and 800 cpi Features	729 II, 729 IV, 729 V, and 7330
1414-2	7330
1414-7	729 II, 729 IV, 729 V, and 729 VI
1414-7 With Intermix Features	729 II, 729 IV, 729 V, 729 VI and 7330

Figure 1. Tape Units Attached to 1414 Tape Synchronizer

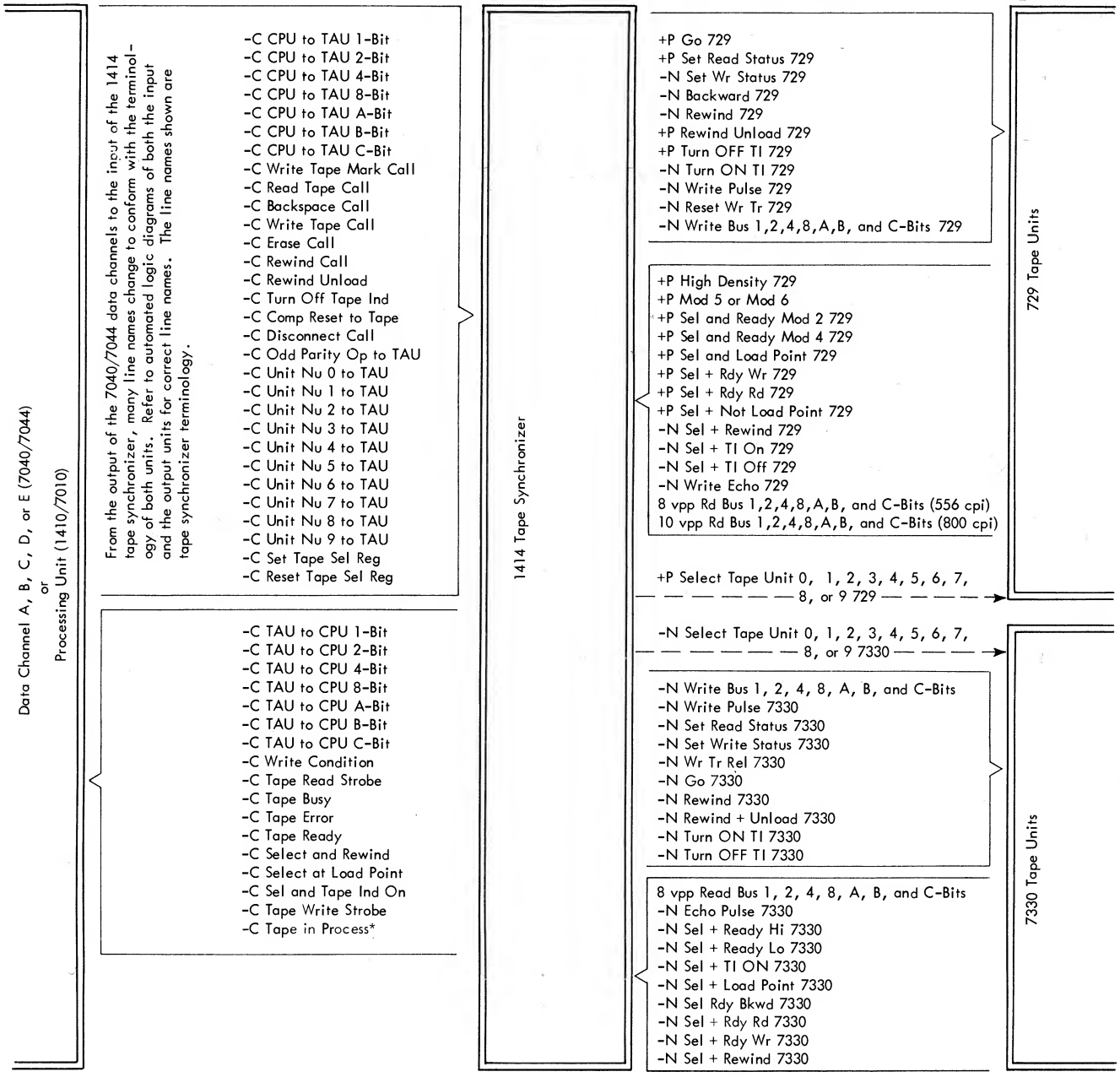
The tape synchronizer processes all signals between the processing unit (1410/7010) or the data channel (7040/7044) and the selected tape unit (Figure 3). Because magnetic tape units are basically tape transport devices with the capacity to read and write characters, the tape synchronizer supplies all timings necessary to execute tape operations. To begin a tape operation, the processing unit (1410/7010) or the data channel (7040/7044) must condition control lines to the tape synchronizer designating a tape unit and the tape operation to be performed. The tape synchronizer assumes control and directs the specified operation. The tape synchronizer has the capacity to store only one character at a time; therefore, the tape synchronizer controls all data transfers between the processing unit or data channel and the selected tape unit.

The 729 II, IV, and 7330 tape units operate at one of two densities, 200 or 556 characters-per-inch (cpi). The 729 V and VI tape units operate at one of three

Tape Unit	729 II		729 IV		729 V			729 VI			7330	
Tape Speed (Inches per Second)	75		112.5		75			112.5			36	
Density (Characters per Inch)	200	556	200	556	200	556	800	200	556	800	200	556
Characters per Second	15,000	41,667	22,500	62,500	15,000	41,667	60,000	22,500	62,500	90,000	7,200	20,016
Average Tape Access Time (Milliseconds)	10.8		7.3		10.8			7.3			20.8	
Character Time (Microseconds per Character)	67.2	24	44.7	16	67.2	24	17	44.7	16	11	139	50

Figure 2. Magnetic Tape Unit Characteristics

densities, 200, 556, or 800 characters-per-inch (cpi). Changing the operating density of a tape unit is a manual operation. Because 729 II, IV, and 7330 tape units record characters at only two densities, the HIGH-LOW density switch setting on the selected tape unit determines the operating density. In high density, 729 II, IV, and 7330 tape units read or write characters at 556 cpi; in low density, these tape units operate at 200 cpi. A three-position tape density switch for each channel to which a tape synchronizer is attached is installed on the operator's console for density selections on 729 V and VI tape units. The positions of the controlling tape density switch and the HIGH-LOW density switch on the 729 V or VI tape unit determine the density at which the 729 V or VI tape unit operates. If the appropriate console tape density switch is in the high position, the HIGH-LOW density switch on the tape unit selects either 800 cpi (high) or 556 cpi (low) operation. If the console tape density switch is in the low position, the HIGH-LOW density switch on the unit selects 556 cpi (high) or 200 cpi (low) operation. The center position of the console tape density switch allows the HIGH-LOW density switch on the 729 V or VI tape unit to select 200 cpi (low) or 800 cpi (high) operation. The console tape density switches do not affect density selections for 729 II, IV, or 7330 tape units.



* 1410/7010 Operation Only

Figure 3. Tape Synchronizer-System Relation

The three magnetic tape operations are read, write, and unit control. In a tape read operation, the selected tape unit reads characters from magnetic tape and transfers data through the tape synchronizer to core storage. In a tape write operation, the selected channel transfers characters through the tape synchronizer to the designated tape unit; the tape unit records characters on magnetic tape. A tape unit control instruction specifies one of five tape operations: rewind, rewind and unload, backspace, write blank tape, or write end of file. Only tape read and write operations require data transfers between core storage and a magnetic tape unit. The IBM 7040 and 7044 Data Processing Systems either use data channels and tape synchronizers as intermediate units between core storage and the selected tape unit (Figure 4) or direct tape operations to an on-line IBM 1401 Data Processing System. A tape synchronizer is not used when a 1401 system controls the tape operation.

Instructions to the processing unit initiate all magnetic tape operations. The instructions specify:

1. The data channel and the tape unit.
2. A tape operation.

If the instruction designates the tape read or write operation, the instruction must also supply the following information to the channel.

3. The starting core storage address.
4. The number of words to be processed to (input) or taken from (output) storage.
5. Binary or BCD mode.

The processing unit assigns system control of the input-output (I-O) operation to the data channel that the tape instruction specifies.

Data Channel Tape Operation

IBM 7040/7044 Data Processing Systems use the command word technique to pass control of I-O operations from the central processing unit (CPU) to data channels. The channels perform such functions as word counting, address modification, assembly of bytes

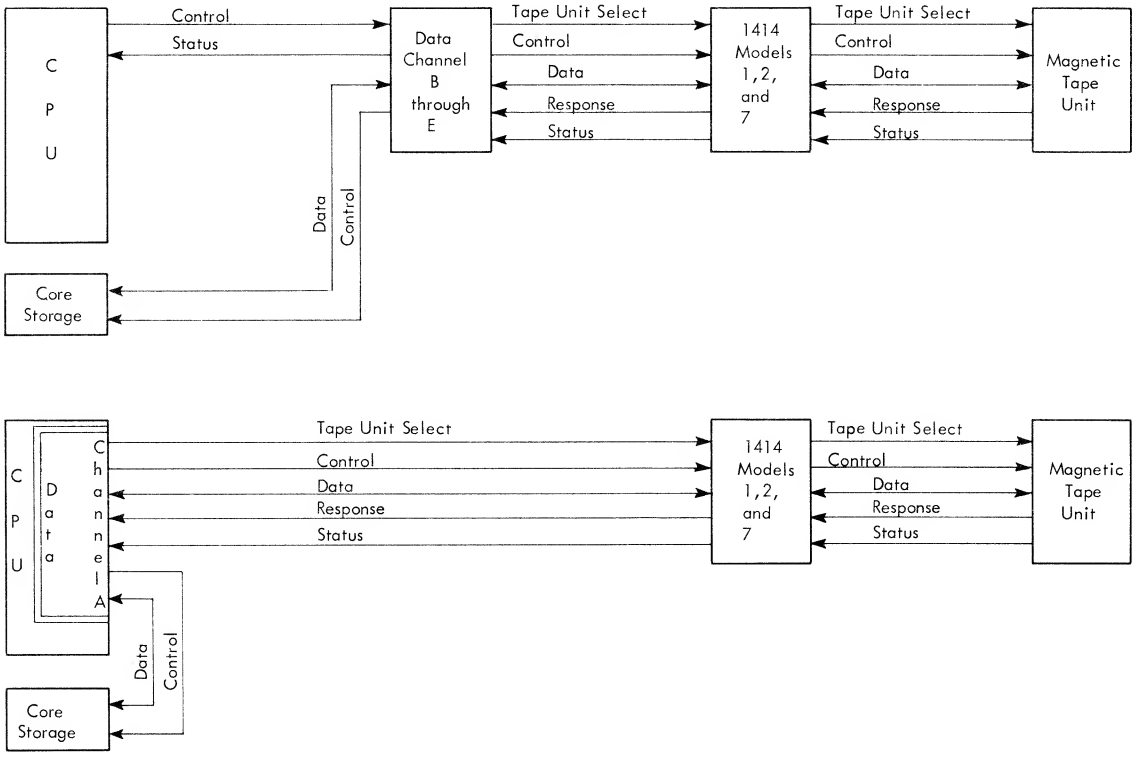


Figure 4. 7040/7044 Tape Operation Data Flow

(characters) into CPU words, disassembly of words into bytes, code translation, and parity assignment and checking.

Data Channel A Tape Operation

Data channel A uses CPU registers and data paths to perform I-O control functions (Figure 5); therefore, channel A tape and CPU operations cannot be overlapped.

The CPU starts an I-O operation when it decodes a select instruction. The output of the channel A interface decoder selects the interface and unit that the instruction designates. Execution of the select instruction is not completed until the I-O unit is in ready status. When selection is complete, the channel terminates select operation, and CPU decodes the next instruction. Normally, the reset and load channel A (RCHA) instruction follows the select instruction to specify the core storage location in which the channel command is stored. When CPU executes the RCHA instruction, it places the channel command in the accumulator register (AC). The command specifies the number of words to be either transmitted or received and the address of the storage position in which the first word is to be stored or from which the first word is to be taken. The shift counter is set to six. When a word (36 bits) is processed:

1. The address part of the command word (AC positions 21-35) is modified to indicate the next sequential storage position.
2. The shift counter (decreased by one each time that six bits are processed on the channel) is reduced to zero.
3. The word counter is decreased by one.

If the word count is not reduced to zero when a complete word is processed, the address part of the command word transfers to the address register (AR), the shift counter is reset to six, and the channel receives or transmits another word. If the word count is zero, the channel ends execution of the RCHA instruction.

READ OPERATION

The tape synchronizer sends seven bit characters (six data bits and check bit) to channel A. The channel removes the check bit and tests the character (byte) for a parity error. A parity error causes the channel redundancy check indicator to turn on, but the read operation continues. Depending on the mask controlling trapping, the channel may or may not transmit succeeding words to core storage. If no parity error is detected, the six data bits are set in the multiplier-quotient register (MQ) in positions 30-35; the shift counter, set to six at the beginning of the operation, is reduced by one, and bits in the MQ are shifted left six positions. When the tape synchronizer transfers the next data byte to the channel, the channel loads the six data bits in MQ positions 30-35, reduces the shift counter by one, and shifts bits in the MQ left six positions. The channel loads six bit bytes in the MQ until the shift counter is reduced to zero, indicating that a complete word has been assembled. The word in the MQ is placed in the storage register to be transferred to the location that the AR specifies; a check bit is then assigned to the storage register. The address count is increased by one to indicate the address of the storage position into which the next word will be loaded. The word count is decreased by one. If the word count is not zero after the reduction, the shift counter is again set to six, and channel A assembles the next word from tape synchronizer bytes. If the word count is set to zero, the channel does not write more characters in core storage, but the tape synchronizer continues to make characters available to the channel until the tape unit reads the complete record. When the tape unit reads the last character in the record and the tape synchronizer completes checks on the record written, the tape synchronizer signals the channel that the read operation is complete. Channel A terminates operation on the RCHA instruction and disconnects the tape synchronizer. The channel also ends operation on the RCHA instruction if the tape synchronizer signals the channel that the read operation is complete before the word counter is decreased to zero.

WRITE OPERATION

The word in the core storage location that the AR designates is set in the MQ. Data bits in MQ positions S, 1-5 transfer to parity generating circuits where a check bit is added to the six data bits if the tape record is to be written in odd parity. The channel then transmits the byte to the tape synchronizer. Bits in the MQ are shifted left six positions; the shift counter, set to six earlier in the operation, is reduced to zero, indicating that a 36-bit word has been disassembled and transferred to the tape synchronizer. While the word is being disassembled, the channel performs command modification by setting the address in the adders, incrementing the address by one, and returning the address to the AC (positions 21-35). During disassembly, the word count (AC positions 3-17) is reduced by one. If the word count is not zero after the reduction, the address transfers to the AR; the shift counter is reset to six when the tape synchronizer accepts the complete word. If the word count is zero, the channel ends operation on the RCHA instruction and disconnects the tape synchronizer when the complete word is transferred.

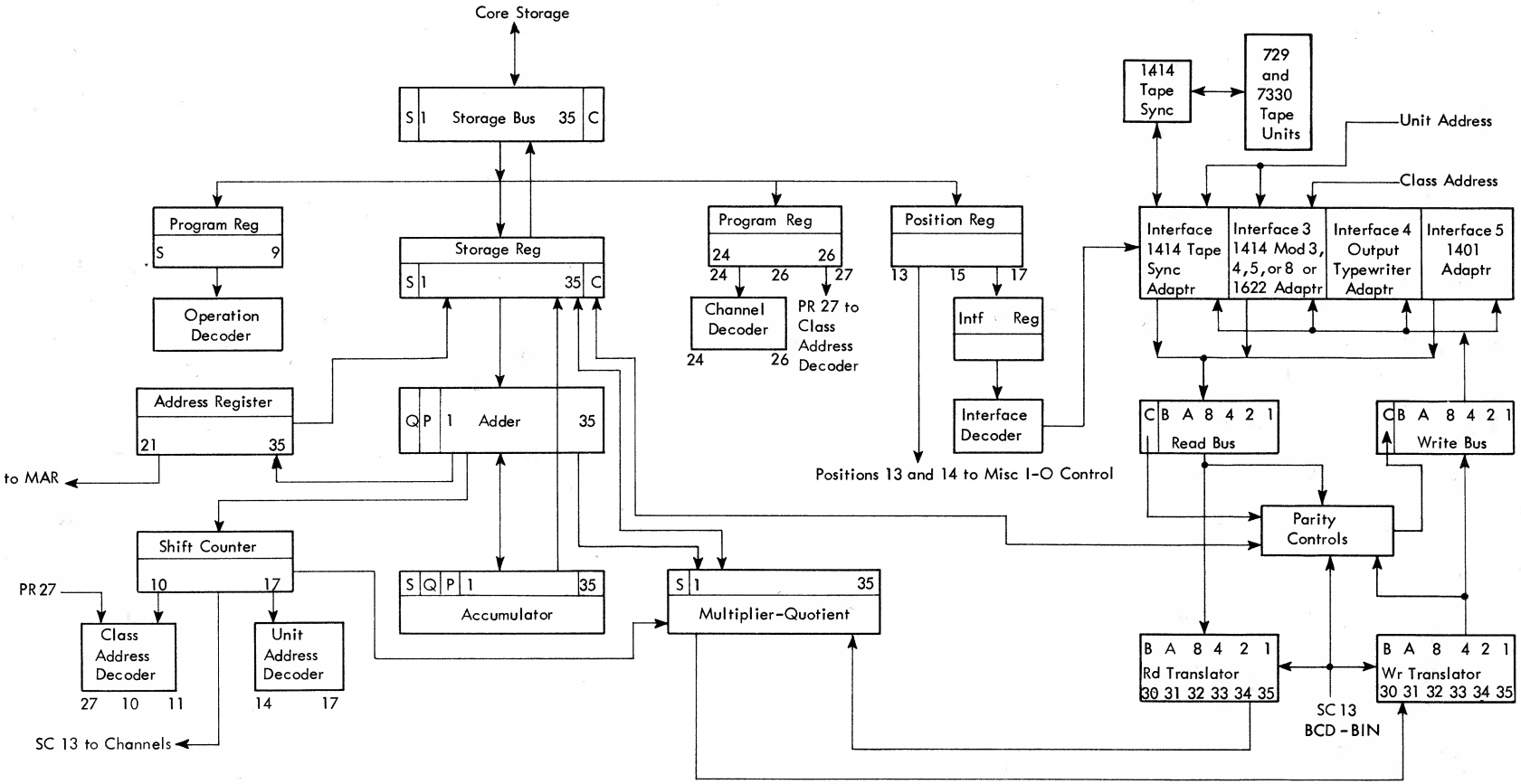


Figure 5. Data Channel A

IBM 7904 Data Channel Tape Operation

The IBM 7904 Data Channel is attached to the 7040/7044 systems as channels B, C, D, and E. Each 7904 data channel contains registers which allow channels B through E to perform I-O control operations independent of the CPU (Figure 6). A description of 7904 data channel registers used in tape operations is as follows:

Data Register: The 37-bit position data register is a buffer between core storage and the assembly register. The data register accepts inputs from the storage bus and the assembly register. In magnetic tape operations, the data register is similar in function to the channel A storage register.

Word Counter: The 15-position word counter indicates the number of words to be processed in the tape operation. Bits loaded in the word counter transfer from the storage bus through the data register. The word counter is decreased by one as each word is processed.

Address Counter: The 15-position address counter indicates the address of the core storage location into which the next word will be stored or from which the next word will be unloaded. Data from the storage bus

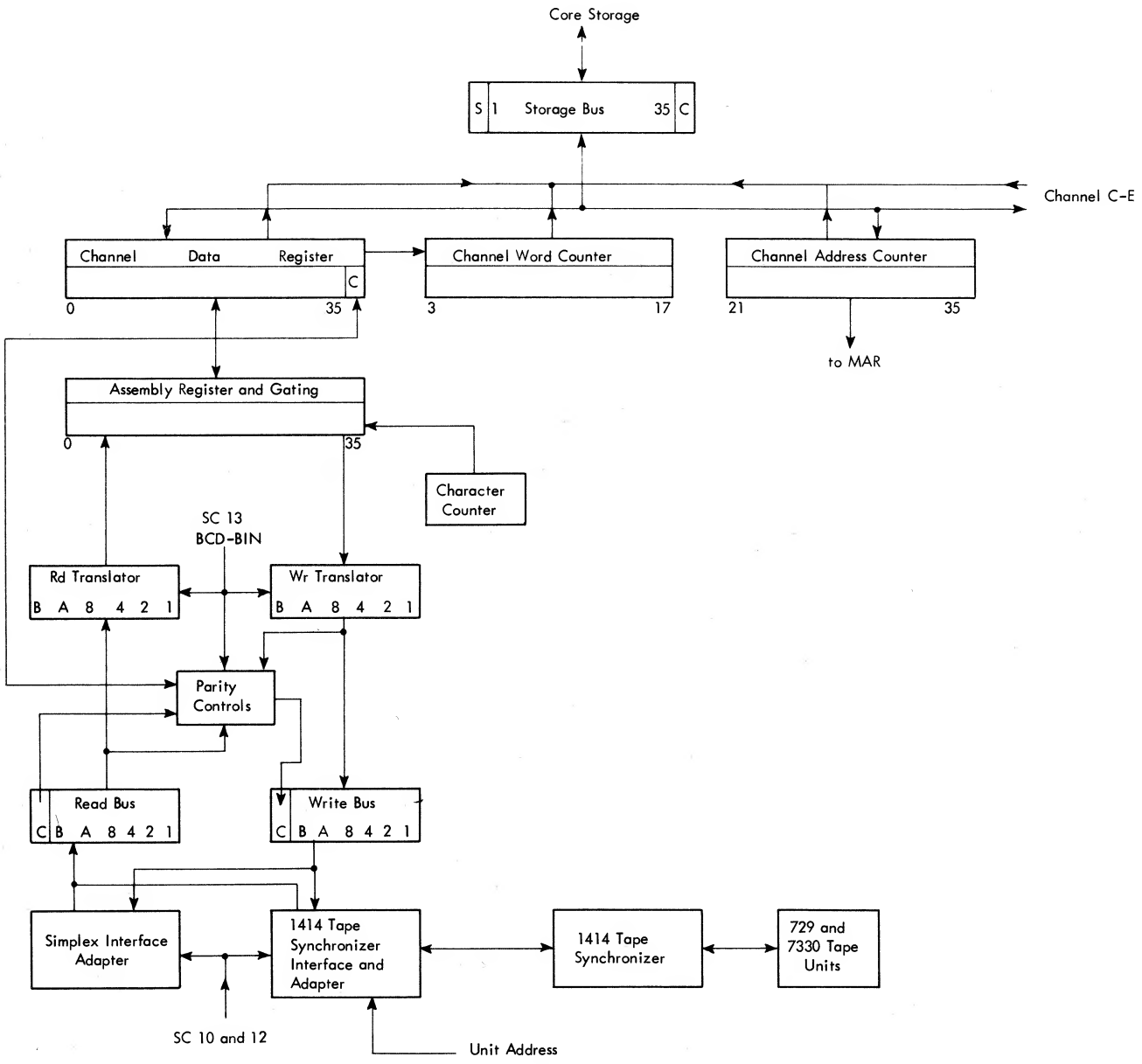


Figure 6. Data Channel B (with Tapes)

loads the address counter. The address counter is increased by one as each word is processed.

Assembly Register: The 36-position assembly register is a buffer between the data register and the tape synchronizer. The assembly register assembles and disassembles words in tape operations in channels B through E as the MQ assembles and disassembles words in channel A tape operations. A character counter in the 7904 data channel selects one of six character positions in the assembly register to be loaded or unloaded in one parallel operation. Like the shift counter in Channel A, the character counter steps six times for each CPU word (once for each six bit byte). However, characters are processed directly from their assembly register positions; bits in the assembly register are not shifted.

The 7904 data channel performs tape operations in basically the same manner as data channel A executes the operations. The outstanding difference is that CPU registers are not used with the 7904, and, therefore, the CPU and the 7904 data channels can operate independently (Figure 6). Even when all 7904 data channels are executing I-O operations the CPU is only required to transfer words to or from core storage. When channel A is in use, CPU cannot perform a different operation since the CPU and channel A share the same registers. However, four 7904 data channels and data channel A can perform I-O operations simultaneously.

Select Instructions

Select instructions effect the selection and control of I-O devices. All select instructions accomplish the following functions.

1. Bit positions 24 through 30 and 32 through 35 in select instructions identify the I-O unit or buffer and the data channel to perform the operation.

2. When required, bit position 31 in a select instruction specifies the appropriate code translator to allow automatic translation from one form of BCD coding to another form of BCD coding.

3. When data channel A performs the I-O operation, bit positions 15, 16, and 17 identify the interface to be used.

4. Bit positions S, and 3 through 11 determine whether the I-O operation is input (from I-O to core storage) or output (from core storage to I-O).

5. Select instructions prepare the data channel to accept the channel command word (IORD); a subsequent reset and load channel (RCH) instruction causes the command word to transfer to the channel.

6. When a select instruction designates a magnetic tape operation, the instruction initiates action to start tape movement on the specified tape unit. Figure 7 shows addresses of magnetic tape units on data channels. Figure 8 shows a breakdown of the address part of select instructions.

Channel	Interface	BCD Mode Addresses		Binary Mode Addresses	
A	O	01201	01212	01221	01232
B	N/A	02201	02212	02221	02232
C	N/A	03201	03212	03221	03232
D	N/A	04201	04212	04221	04232
E	N/A	05201	05212	05221	05232

Figure 7. Addresses of Magnetic Tape Units on Data Channels

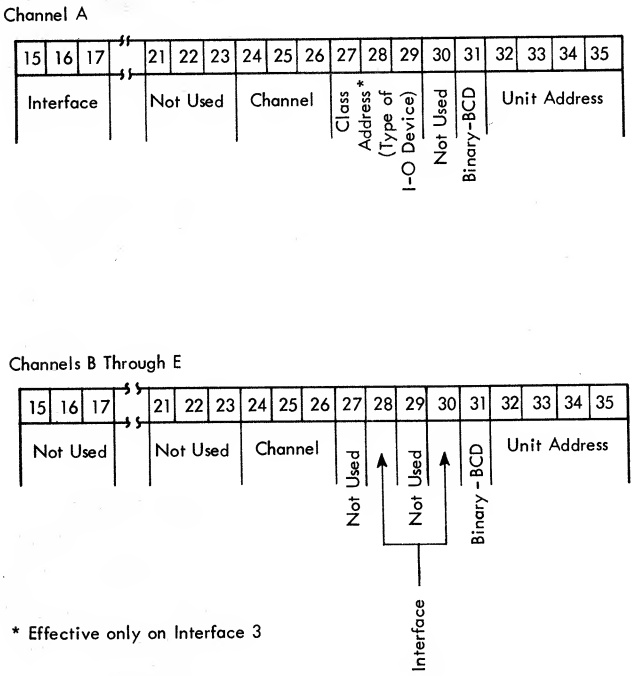


Figure 8. Breakdown of Address Part of Select Instruction

Ten tape unit select lines are routed from the data channel to the tape synchronizer. To permit the synchronizer to perform unit control instructions independent of channel control, the channel checks to determine if the tape synchronizer is busy before resetting the previous I-O operation and selecting a new tape unit.

Translation

Because magnetic tape units can read and write in binary or BCD mode, the address part of the select instruction must specify BCD or binary operation. A zero in bit position 31 of the select instruction designates BCD mode; a one in bit position 31 designates binary mode.

When the tape synchronizer transfers 7-bit BCD characters to the channel, zone bits in some characters

are altered so that characters A through Z are represented in core storage by 6-bit binary numbers of increasing magnitude. Altered zone bits are shown in Figure 9.

Six-bit binary numbers 000 001 through 001 001 represent digits 1 through 9; the zone part of the digits is 00. The digit zero is represented on tape by the bit configuration 001 010; the bit configuration 000 000 represents the digit zero in core storage. The read translator in the data channel alters characters in BCD read operations so that their codes are compatible with the unit to which they are being transferred. During a BCD write operation, the write translator in the data channel translates core storage characters into tape BCD form.

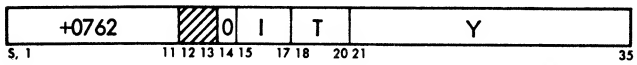
Class	In Core Storage		On Tape	
	B	A	B	A
Numeric	0	0	0	0
A Through I	0	1	1	1
J Through R	1	0	1	0
S Through Z	1	1	0	1

Figure 9. Zone Bit Alteration

Read, Write, Sense, and Control Select Instructions

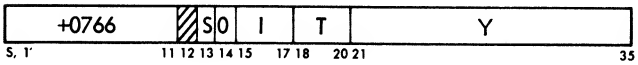
If the channel-in-use indicator is on when CPU decodes a read, write, sense, or control select instruction, execution of the instruction is delayed until the channel-in-use indicator is turned off. A WRS, WBT, or WEF, to a file protected tape unit on overlap channel hangs-up the selected channel (channel-in-use stays on).

Read Select (RDS)



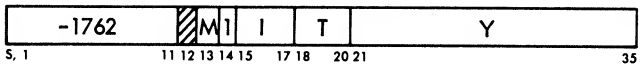
The read select instruction conditions the designated data channel to receive data from the I-O device that I and Y specify; the channel processes data from the I-O unit to core storage. Only bit positions 28 through 35 are subject to effective address modification; bit position 14 must contain a zero.

Write Select (WRS)



The write select instruction conditions the designated data channel to transmit data from core storage to the I-O device that I and Y specify. Only bit positions 28 through 35 are subject to effective address modification; bit position 14 must contain a zero.

Sense Select (SEN)



The sense select instruction conditions the designated data channel to transmit status data from the I-O device that I and Y specify to core storage. Only bit positions 28 through 35 are subject to effective address modification; bit position 14 must contain a one. The sense select instruction causes a store and trap on 7090/7094 systems. If the select instruction addresses a device in BCD mode, no translation occurs.

When an RCH instruction loads the channel with an IORD command with a word count greater than zero and follows a sense select instruction, the channel stores the following sense data in character position zero (Bits S, 1 through 5) of the first word.

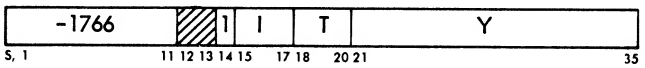
S-bit (B-bit) not ready

3-bit (4-bit) rewinding (not ready indication is also given)

5-bit (1-bit) load point

In real time or teleprocessing applications, it is possible to lose information if the system cannot respond to an interrupt signal soon enough. The 7040/7044 systems select instructions have undesirable features in that they cause CPU to hang up if a *not ready* tape unit is selected. In order to minimize the hang up hazard, the sense select instruction is used to ascertain the ready status of a selected I-O device. The sense select instruction will not cause CPU to hang up if the channel is not in use, even if the addressed I-O device is not ready. A sense select instruction hangs up CPU if a non-existent channel is specified.

Control Select (CTR)



The control select instruction conditions the channel to transmit control data from core storage to the I-O device that I and Y specify. Only positions 28 through 35 are subject to effective address modification; bit position 14 must contain a one. The control select instruction causes a store and trap on the 7090/7094 systems.

Although the control select instruction is not normally used with magnetic tapes, it initiates the same action that the write blank tape instruction causes.

Channel Control Instructions

When a select instruction has conditioned the channel to transmit data to or from an I-O device, a reset and load channel (RCH) instruction must be given to deliver the command word to the channel. The command word contains a starting core storage address and a word count to control the transmission of data to or from core storage.

Because the select instruction initiates action to start tape movement on the specified tape unit, the RCH instruction must be executed within a definite time after the select instruction has been performed. Maximum times that should elapse between the execution of the select and RCH instructions are shown in Figure 10.

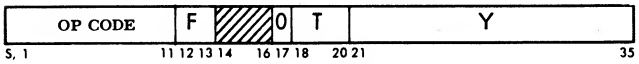
Tape Unit	Read	Write
7330 - I	3.7	6.2
729 - II	4.0	6.5
729 - IV	4.0	6.5
729 - V	2.5	4.0
729 - VI	2.5	4.0

All Timings Are in Milliseconds and Allow for a 10% Variation in 1414 Tape Synchronizers

Figure 10. Maximum Times Between Select and RCH Instructions

In a write operation if either the CPU does not execute the RCH instruction within the specified time or the RCH instruction loads the channel with an IORD command with a word count of zero, the tape unit disconnects, the I-O check indicator turns on, and the channel-in-use indicator turns off. In a read operation, the channel checks parity for the entire tape record even if an RCH instruction is not given.

Reset and Load Channel Instruction (RCH)



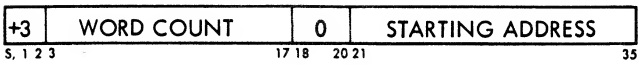
MNEMONIC	OP CODE	CHANNEL
RCHA	+0540	A
RCHB	−0540	B
RCHC	+0541	C
RCHD	−0541	D
RCHE	+0542	E

If a select instruction has conditioned the channel, the contents of Y, C(Y), transfer to the channel as a command word; the channel can then transmit data to or from the selected I-O device. If a select instruction has not conditioned the channel, the I-O check indicator turns on; the C(Y) are sent to the channel as a command word, but transmission does not occur.

If a second RCH instruction is given to a channel already in operation, the C(Y) transfer to the channel and replace the previous command word. Transmission continues with the new address and word count. A second RCH instruction cannot be issued to channel A; overlap operation cannot occur on channel A.

Because timings vary between the data channels on the 7040/7044 systems and the data channels on the 7090/7094 systems and between the overlap and non-overlap channels on the 7040/7044 systems, the selected channel should be tested to be sure that it is no longer in use prior to using the data area assigned to the channel. This test can be performed by executing a TCOX instruction.

Input-Output of a Record and Disconnect (IORD) Command



Execution of the RCH instruction causes the channel command word (IORD) to transfer to the channel to control the tape operation. The IORD command word provides:

1. a 15-bit word count that specifies the number of words to be transferred between core storage and the tape unit.

2. a 15-bit starting address that specifies the location in core storage for the first word of the record. Additional words are taken from or sent to successively higher locations in storage until either the I-O device reads the end of the record or the number of words specified in the word count have been transmitted.

The 7040/7044 systems do not interpret positions S, 1, 2, 18, 19, and 20 when the IORD is used as a channel command word.

The IORD may appear at any point in the program. If the IORD transfers to the CPU operation decoder as an instruction word (during I cycle), the IORD is interpreted as a TXH instruction because of the +3 prefix. A TXH instruction with no index register specified causes no operation; the next sequential instruction is performed. Thus, the CPU processes an IORD with a prefix of +3 and a tag of zero as an NOP instruction.

Tape Control Instructions

If the channel-in-use indicator is on when CPU decodes a unit control instruction (write end of file, write blank tape, backspace record, rewind, or rewind unload), execution of the instruction is delayed until the channel-in-use indicator turns off. A unit control instruction or a select instruction turns on the designated channel's channel-in-use indicator. The channel-in-use indicator turns off when the specified I-O operation is completed.

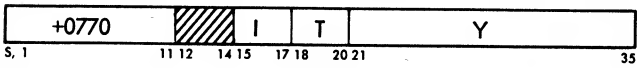
Tape Data Compatibility

If the first character of a BCD tape record is a tape mark (8, 4, 2, and 1-bits) in the 7090/7094 systems, the tape mark and the following character are replaced by zeros, and the redundancy check indicator is set. If the first character of a BCD tape record is a tape mark in the 7040/7044 systems, all characters are received properly, and the redundancy check indicator is not set. For example, if the first six characters of a BCD tape record are √ABCDE, the following word appears in core storage after the tape read operation.

7040/7044	√ABCDE
7090/7094	00BCDE ----------the redundancy check indicator lights.

Tape marks should not be written as the first characters of BCD records for 7090 program compatibility considerations.

Write End-of-File (WEF) Instruction



The write end of file instruction causes the channel to condition the write tape mark call and erase call lines to the tape synchronizer. The selected tape unit erases a 3¾ inches end of file gap and writes a tape mark (with the check character) on tape (Figure 11). The 3¾ inches end of file gap is required for compatibility with the IBM 7040 Data Processing System when operating in binary mode. An end of tape reflective spot encountered during execution of the WEF instruction turns on the end of tape indicator. Only positions 28 through 35 of the address part of the instruction are subject to effective address modification.

Write Blank Tape (WBT) Instruction

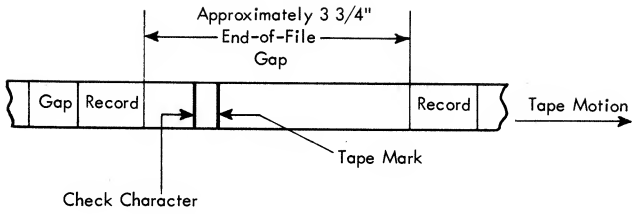
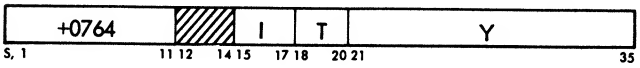


Figure 11. End-Of-File-Gap

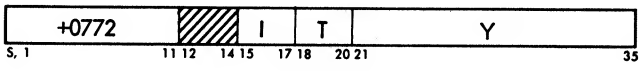
The write blank tape instruction causes the channel to condition "erase call" and then "write call" to the tape synchronizer. The selected tape unit erases a section of tape approximately 3¾ inches in length. The WBT instruction is used to space over bad spots on tape that cause redundancy checks. An end of tape reflective spot encountered during execution of the WBT instruction causes the end of tape indicator to turn on. The 7090/7094 systems execute a write blank tape operation when a write select (WRS) instruction not followed by a reset and load channel (RCH) instruction is detected. Because the 7090/7094 Systems decode the 7040/7044 WBT instructions as a WRS instruction, an RCH instruction should not follow a WBT instruction for 7090/7094 program compatibility. If a subsequent RCH instruction is given, the IORD command should specify a zero word count.

Backspace Record (BSR) Instruction



The backspace record instruction causes the channel to condition "backspace call" to the 1414 tape synchronizer. The selected tape unit moves tape backward through one tape record or to load point; tape movement stops when either the interrecord gap or load point is sensed. The tape synchronizer performs no checks during execution of the backspace operation. If the selected tape unit is at load point when the BSR instruction is given, no operation occurs. Only bit positions 28 through 35 of the address part of the instruction are subject to effective address modification.

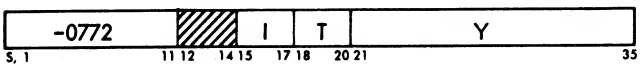
Rewind (REW) Instruction



The rewind instruction causes the channel to condition "rewind call" to the 1414 tape synchronizer. The

selected tape unit rewinds tape to the load point position. If tape is positioned at load point when the tape synchronizer receives "rewind call," no operation occurs. Only bit positions 28 through 35 of the address part of the REW instruction are subject to effective address modification. When a 7330 tape unit is selected to perform the operation, the REW instruction causes the tape unit to rewind tape at low speed regardless of the amount of tape on the machine reel.

Rewind and Unload (RUN) Instruction



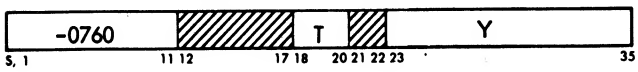
The rewind and unload instruction causes the channel to condition "rewind unload call" to the 1414 tape synchronizer. The selected tape unit rewinds tape to the load point position and unloads tape. When a 7330 tape unit is selected to perform the operation, the RUN instruction causes the tape to unload and rewind tape at high speed. If a 7330 tape unit is at load point when the channel conditions "rewind unload call" to the tape synchronizer, the RUN instruction "hangs up" the channel. If a 729 tape unit is at load point when the channel issues "rewind unload call" to the tape synchronizer, the tape unit performs an unload operation.

Channel Instructions That Apply Only To Magnetic Tapes

End of Tape Indicator

When the tape unit senses the reflective strip marking the end of tape in a write, write end of file, or write blank tape operation, the end-of-tape indicator in the channel turns on. The tape operation is not interrupted; writing can be completed even though the end of tape marker has been sensed. If CPU initiates another operation causing tape to move forward, tape may be pulled from the file reel. The end-of-tape indicator is not turned on during a read operation.

End of Tape Test (ETTX) Instruction



The end of tape test instruction tests the status of end-of-tape indicator on the data channel that the address part of the instruction specifies. Addresses for the channels are:

Channel A	01000
Channel B	02000
Channel C	03000
Channel D	04000
Channel E	05000

If the end-of-tape indicator for the specified data channel is on, execution of the end of tape test instruction turns the indicator off; CPU performs the next sequential instruction. If the indicator is off, the instruction causes CPU to skip the next instruction and execute the second instruction in sequence.

Other Applicable Instructions

Redundancy Check Indicator

The channel redundancy check indicator can be turned on at any time during a tape read or write operation by one of the following tape synchronizer error conditions:

- Read/write register VRC error
- Longitudinal redundancy check register error
- Skew error (write operation)
- Write compare error (write operation)
- Write echo error (write operation)
- Read register A VRC error (write operation)
- Write delay noise (write operation)

The data channel turns on the redundancy check indicator if it detects a parity error in the data received in a read or sense operation.

Transfer on Redundancy Check (TRCX) Instruction

If the redundancy check indicator for the specified channel is on, execution of the TRCX instruction turns off the indicator, and the CPU takes the next instruction from location Y. If the indicator is off when the CPU executes the TRCX instruction, the CPU performs the next instruction in sequence. If the channel parity enable mask bit is set to one, the TRCX instruction is not effective; execution of the instruction does not turn off the redundancy check indicator, and no transfer is taken if the indicator is on. The instruction designates data channels in the following manner.

TRCA	+0022	Transfer on channel A redundancy check
TRCB	−0022	Transfer on channel B redundancy check
TRCC	+0024	Transfer on channel C redundancy check
TRCD	−0024	Transfer on channel D redundancy check
TRCE	+0026	Transfer on channel E redundancy check

End of File Indicator

When the tape unit reads a single character tape mark record during a channel tape read operation, the channel end of file indicator turns on and disconnects the tape synchronizer through a normal read disconnect (EOR). The end of file indicator does not turn on when a tape mark (end of file character) is written on tape.

Transfer on End of File (TEFX) Instruction

If the end of file indicator for the specified data channel is on, the transfer on end of file instruction turns off the indicator and causes CPU to execute the instruction in core storage location Y. If the indicator is off, the transfer on end of file instruction causes the CPU to execute the next sequential instruction. The instruction designates data channels in the following manner.

TEFA	+0030	Transfer on channel A end of file
TEFB	−0030	Transfer on channel B end of file
TEFC	+0031	Transfer on channel C end of file
TEFD	−0031	Transfer on channel D end of file
TEFE	+0032	Transfer on channel E end of file

If the tape unit senses the end-of-file indication (single character tape mark record) during a read operation, the end of file indicator on the channel turns on and disconnects the tape synchronizer. If the channel operation enable bit is a one, the TEFX instruction does not cause a transfer or turn off the end of file indicator.

Channel In Use Indicator

The channel in use indicator on each data channel is turned on when any select instruction or tape unit control instruction specifies that channel to perform an operation. The indicator is turned off when the designated operation is completed. If an RDS, PRD, WRS, PWR, SEN, CTR, BSR, WEF, REW, RUN, or WBT instruction is given while the channel in use indicator is on, execution of the new instruction is delayed until the previous operation is terminated and the channel in use indicator is turned off.

Transfer on Channel in Operation (TCOX) Instruction

If the channel-in-use indicator for the specified channel is on when the CPU executes the TCOX instruction, the CPU performs the instruction in location Y. If the channel-in-use indicator is off, the CPU performs the next sequential instruction. The TCOX instruction does not effect channel operation. The instruction designates data channels in the following manner.

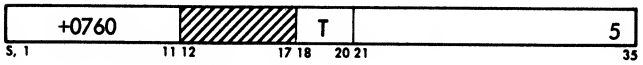
TCOA	+0060	Transfer on channel A in operation
TCOB	+0061	Transfer on channel B in operation
TCOC	+0062	Transfer on channel C in operation
TCOD	+0063	Transfer on channel D in operation
TCOE	+0064	Transfer on channel E in operation

Input-Output Check Indicator

The I-O check indicator on the console turns on when:

1. An RCHX instruction is decoded, and the designated channel is not selected.
2. An IORD command with a zero word count follows a write select instruction to tape.
3. Write gate is inactive and the tape synchronizer has conditioned "write condition." This condition results when an RCHX instruction is not given soon enough; the tape synchronizer is reset.
4. The channel (B through E) data register or channel A storage register has not been loaded with a word from core storage by the time that its contents are to be sent to an output unit.
5. The channel (B through E) data register or channel A storage register has not transmitted its contents to core storage by the time that new data are available to be loaded in the register.

Input-Output Check Test (IOT) Instruction



If the I-O check indicator is on when CPU executes the IOT instruction, the indicator turns off, and CPU performs the next sequential instruction. If the indicator is off, CPU skips the next instruction and performs the second instruction in sequence. Because the address in the instruction is part of the op code, any address modification may change the operation.

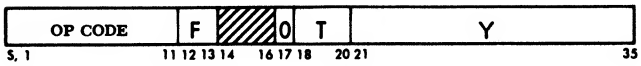
Reset Data Channel (RDCX) Instruction

The reset data channel instruction resets all registers and indicators in the specified data channel (except in Channel A, the accumulator and MQ registers are not cleared). The channel terminates the I-O operation and disconnects the tape synchronizer immedi-

ately. If the instruction is executed while tape is in motion, tape movement stops regardless of the position of the tape head with respect to the interrecord gap. If the tape unit is rewinding tape, the rewind operation is completed. Status indicators previously set by an enable instruction are reset. The RDC instruction cancels the effect of a previous select instruction. The instruction designates data channels in the following manner:

MNEMONIC	OP CODE	ADDRESS	COMMENT
RDCA	+0760	01352	Reset data channel A
RDCB	+0760	02352	Reset data channel B
RDCC	+0760	03352	Reset data channel C
RDCD	+0760	04352	Reset data channel D
RDCE	+0760	05352	Reset data channel E

Store Channel (SCHX) Instruction



The store channel instruction replaces the contents of Y (bit positions 21-35) with the contents of the specified channel address counter. The contents of the channel word counter replace the contents of bit positions 3-17; bit positions S, 1, 2 and 18 through 20 are destroyed. Because channel A uses accumulator bit positions 3-17 for the word counter and 21-35 for the address counter, it is necessary to execute the store channel A instruction before changing the accumulator after a reset and load channel A instruction. Note, however, on channel A, bits 1-35 of accumulator are stored. A store channel instruction designating channels B through E can be executed even though the specified channel is in operation. If the channel is busy and the channel address register is in the process of changing, execution of the store channel instruction is delayed until the change is complete.

The address register is one greater than the storage location of the last word loaded in or taken from core storage. The instruction designates data channels in the following manner.

SCHA	+0640	Store channel A
SCHB	−0640	Store channel B
SCHC	+0641	Store channel C
SCHD	−0641	Store channel D
SCHE	+0642	Store channel E

Channel Traps

A data channel can interrupt CPU processing by trapping the CPU program. One of many conditions can initiate a channel trap; conditions that apply to magnetic tape are as follows:

1. The completion of any channel operation
2. A redundancy check
3. An end of file (single character tape mark record)
4. A word parity check during a U or B cycle
5. An incomplete tape word (corporate interface unusual end)

When a channel trap occurs, the contents of the instruction counter are stored in the address portion of the store location. Bits indicating the conditions that caused the trap are loaded in the decrement section of the store location; other bits in the store location are destroyed. The CPU transfers to the instruction location for the next instruction; for 7090/7094 compatibility, the instruction should be an unconditional transfer. Store locations and instruction locations are as follows:

CHANNEL	STORE LOCATION	INSTRUCTION LOCATION
A	00012	00013
B	00014	00015
C	00016	00017
D	00020	00021
E	00022	00023

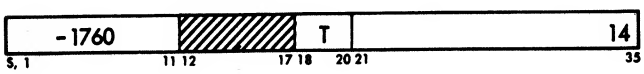
A channel trap cannot occur if an executed trap or an inhibit channel traps instruction has reset the channel trap control.

Enable (ENB) Instruction

Execution of each enable instruction cancels the effect of previous enable instructions and sets the channel mask bits to one or zero as indicated by the contents of Y. The enable instruction turns on channel trap control. Execution of a trap or inhibit channel traps instruction prevents further traps until CPU executes another enable or restore channel trap instruction. When either the reset or clear key is pressed or CPU executes a reset data channel instruction, all mask bits in the channel are set to zero.

ENB ZERO disables all channel and direct data traps and prevents the location of word parity errors in memory by use of the store channel instruction when a parity error occurs on a channel write operation. Therefore, the inhibit channel traps instruction should be used when necessary to prevent channel traps.

Inhibit Channel Traps (ICT) Instruction



The inhibit channel traps instruction turns off channel trap control, inhibiting all channel traps and direct data traps until a new ENB or restore channel traps instruction is given. Because the address part of the instruction is part of the operation code, any address modification may change the operation.

Restore Channel Traps (RCT) Instruction

The restore channel traps instruction turns on channel trap control, allowing traps to occur as specified by the previous enable instruction. The RCT instruction cancels the inhibiting effect of an executed channel trap or ICT instruction. The address in the instruction is part of the operation code; any address modification may change the operation.

Channel Trap Stores

When a channel trap occurs, the condition(s) causing the trap are stored in the decrement part of the store location. Because more than one condition can set its bit position to a one simultaneously, all positions should be checked. Bit positions applicable to tape operations are:

BIT POSITION IN THE STORE LOCATION	INDICATOR	MASK BIT NAME
17	Operation complete	Operation
16	Redundancy check	Parity
15	End of file	Operation
14	Word parity	Parity or Operation
12	Unusual end (tape word incomplete)	Operation

OPERATION COMPLETE

Bit 17 (operation complete) is turned on when the channel in use indicator changes from the on to the off state; this occurs either at the completion of every read, write, sense, and control operation (end of data transfer), or when the magnetic tape unit completes a BSR, WBT, or WEF operation or begins a REW or RUN operation. Even though bit 17 is stored when the indicator is on and a trap occurs (other conditions may be stored by the same trap), a TCOX instruction can be used to determine the status of the channel.

REDUNDANCY CHECK

Either a parity error from the I-O device or a byte parity check in the channel turns on bit 16 (redundancy check). When the channel X parity mask bit is zero, a TRCX instruction can test and reset the redundancy check indicator. When the channel X parity mask bit is one, execution of the TRCX instruction does not transfer or turn off the indicator. When the parity mask bit is one and the redundancy check indicator is on, the channel stops the transfer of data to or from storage. The channel address register contains one plus the address of last word transferred. A trap or store operation does not occur if the channel is in use. In tape read operations, the designated data channel is in use while the tape unit reads the entire record even when data is not transferred to core storage. The parity bit masks the redundancy check indicator.

END-OF-FILE

The end-of-file signal from the tape unit sets bit 15 (end-of-file). When the channel X operation mask bit is zero, a TEFX instruction can test and reset the end-of-file indicator. When the operation mask bit is one, execution of the TEFX instruction does not transfer or turn off the indicator. A trap or store operation does not occur if the channel is in use. The operation mask bit masks the end-of-file indicator.

WORD PARITY

A word parity error during read or write (U or B) cycles to storage turns on bit 14 (word parity). The word parity bit can also be turned on during channel write operations by checking the 37th bit of a word with the sum of the six parity bits of a disassembled word. When the parity mask bit is one and the word parity indicator is on, the channel stops data transfers to or from core storage. The channel address register contains one plus the address of the last word transferred. Therefore, if the parity enable bit is one when an invalid word is taken from core storage during a write operation, an SCHX instruction stores one beyond the address of the invalid word. A trap or store operation does not occur if the channel is in use. When either the parity mask bit or the operation mask bit is one and the channel is not in use, the indicator may signal a trap and store.

NOTE: Two different mask bits can turn on the word parity indicator. The parity mask bit allows the channel to stop transmission when an error occurs, but the operation mask bit does not make this provision.

UNUSUAL END (TAPE WORD INCOMPLETE)

If the total number of characters processed in the tape operation is not a multiple of six, bit 12 [unusual

end (tape word incomplete)] is set at the end of a tape read or write operation.

If the total number of characters in a tape record is not a multiple of six, the record probably contains an error. The unusual end indicator is not set when the tape unit reads the end of file character (tape mark). If this condition occurs while writing tape, a malfunction exists. At the completion of an IORD, the simplex interface unusual end signal can also set the unusual end indicator. The indicator, masked by the operation mask bit, cannot signal a trap while the channel is in use.

1410/7010 Channel Tape Operations

The three magnetic tape operations are: read, write, and unit control. In a tape read operation, the selected tape unit reads characters from magnetic tape and transfers data through the tape synchronizer to core storage. In a tape write operation, the processing unit transfers core storage characters through the tape synchronizer to the designated tape unit; the tape unit records characters on magnetic tape. A tape unit control instruction specifies one of five tape operations: write tape mark, backspace, rewind, rewind unload, or erase. All tape instructions contain an operation code and select:

1. An input-output channel.
2. Overlap or unoverlap operation.
3. A tape unit.
4. A tape operation.
5. Odd or even parity operation.

In addition, tape read and write instructions designate a core storage address into which the first character is stored or from which the first character is taken and the condition(s) to end the operation. All 1410/7010 instructions designating magnetic tape operations are listed in Figure 12.

The processing unit checks the states of the tape synchronizer and the selected tape unit at status sample A time for all tape operations. If either the tape synchronizer is busy or the selected tape unit is not ready, the processing unit terminates the operation and decodes the next sequential instruction. In checking the state of the tape synchronizer, the processing unit examines the level of the tape busy line at I-ring 5 time to determine if the tape select register may be reset at I-ring 6 time. If the tape synchronizer is controlling another operation, the tape busy line prevents de-selecting of the tape unit. The processing unit sets the channel's busy status indicator latch and skips the designated tape instruction. The processing unit loads the channel's unit number register with the character designating the tape unit to perform the operation at I-ring 5 time (Last Logic Gate). The processor resets the tape select register in the tape synchronizer at I-ring 6 time (Logic Gate C), then conditions the tape select register in the tape synchronizer at I-ring 6 time (Last Logic Gate). The unit number register sets the tape select register at I-ring 6 time. The tape select register signals the designated tape unit. If the tape unit is in ready status, the tape unit conditions the select and ready line to the tape synchronizer. The tape synchronizer relays the ready indication to the processor, allowing the operation to proceed. If the selected tape unit is not conditioned to perform a tape operation, the processing unit sets

Character	Position in Instruction	Function
M	Op Code (Read or Write)	I-O Op Code Without Word Marks
or		
L	Op Code (Read or Write)	I-O Op Code With Word Marks
U	Op Code (Unit Control)	
%	X-Field 1	Use E Channel Unoverlap
or		
@	X-Field 1	Use E Channel Overlap
¤	X-Field 1	Use F Channel Unoverlap
or		
*	X-Field 1	Use F Channel Overlap
?	X-Field 1	Use G Channel Unoverlap (7010)
or		
$	X-Field 1	Use G Channel Overlap (7010)
!	X-Field 1	Use H Channel Unoverlap (7010)
or		
#	X-Field 1	Use H Channel Overlap (7010)
U	X-Field 2	Select Tape Operation (Even Parity)
or		
B	X-Field 2	Select Tape Operation (Odd Parity)
0-9	X-Field 3	Select Magnetic Tape Unit
xxxxx	B-Address(Read or Write)	High Order Position of the Field
W	d-Modifier (Write)	Write Tape to Group Mark-Word Mark or to End of Storage
or		
X	d-Modifier (Write)	Write Tape to End of Storage (Unoverlap)
R	d-Modifier (Read)	Read Tape to Group Mark-Word Mark or to End of Storage
or		
$	d-Modifier (Read)	Read Tape to End of Storage (Unoverlap)
B	d-Modifier (Unit Control)	Backspace a Tape Record
E	d-Modifier (Unit Control)	Skip and Blank Tape
M	d-Modifier (Unit Control)	Write a Tape Mark
R	d-Modifier (Unit Control)	Rewind Tape
U	d-Modifier (Unit Control)	Rewind and Unload Tape

Figure 12. Format for Magnetic Tape Instructions

the channel's not ready status indicator latch and decodes the next sequential instruction.

The write tape call, read tape call, or write tape mark call signal to the tape synchronizer causes the tape synchronizer to condition the tape in process and tape busy lines to the processing unit; "call" signals that initiate other tape operations cause the tape synchronizer to condition only the tape busy line. "Tape in process" blocks the set path to the channel's external end of transfer latch, holding the channel committed to the tape operation. "Tape busy" indicates that the tape synchronizer is performing an operation. If an IBM 7330 Magnetic Tape Unit is selected to execute the tape operation, the tape synchronizer cancels "tape in process" to the processing unit before dropping "tape busy"; this allows the processing unit to condition "external end of transfer" and perform status sample B checks while the tape synchronizer is still busy. Another tape operation on the same channel cannot begin, however, until the previous tape operation is complete and the tape synchronizer drops "tape busy".

Sensing the end of tape reflective spot in a tape write operation or reading a tape mark as the first character in the record in a tape read operation causes the tape indicator (TI) light on the selected tape unit to turn on. The tape unit then signals the involved I-O channel with the select and TI on line, causing the channel's condition and turn off tape indicator latches to turn on at status sample B and second sample B respectively. The turn off tape indicator latch gates "turn off TI" to the selected tape unit to turn off the tape indicator light.

The tape synchronizer conditions "tape error" to the processing unit if it detects an error while executing the tape operation. "Tape error" sets the channel's data check status indicator at status sample B time.

Channel Tape Write Operations

In tape write operations, the processing unit transfers characters from core storage to the channel designated by the tape write instruction. Channel circuits process, then hold the character(s) until the tape synchronizer is ready to transfer the data to the selected tape unit. The tape synchronizer controls all data transfers from the channel to the read-write register in the tape synchronizer.

The d-modifier in the tape write instruction determines the condition that causes the processing unit to transmit "disconnect call" to the tape synchronizer, ending the tape write operation. If the d-modifier in the write instruction is W, the processing unit conditions "disconnect call" when either the first group mark word mark in core storage is sensed or the end of storage condition is detected. If the d-modifier is X and the tape write operation is being performed in unoverlap mode, the processing unit conditions "disconnect call" when the end of storage condition is sensed; group mark word marks are processed as normal characters. If the write instruction with the X d-modifier is executed in overlap mode, the first group mark word mark sensed in storage or the end of storage indication causes the processing unit to issue "disconnect call". "Disconnect call" initiates tape synchronizer actions to end the tape write operation.

The E- and F-channels on the 1410 system process characters to the tape synchronizer in the same manner. The 7010 E-, F-, G-, and H-channel actions in tape operations are alike. Figures 13 and 14 show diagrammed E-channel actions in 1410 and 7010 tape write operations.

7010 E-Channel Tape Write Operation

In a 7010 E-channel tape write operation, the processing unit turns on the block command latch at the end of status sample A time to prevent the E-channel from conditioning "write tape call" to the tape synchronizer until the processing unit executes the first E-cycle. The B-address in the write instruction specifies the core storage position containing the first character to be transferred to the processing unit. If the character is a group mark word mark and the d-modifier in the write instruction is W, the processing unit initiates a series of actions that allow the block command latch to remain set and turn on the external end of transfer latch. The group mark word mark on the B-channel sets the internal end of transfer latch. "External end of transfer" and "internal end of transfer" set the status sample B latch. Because the block command latch is on at the end of the first E-cycle, the processing unit does not condition "write tape call" to the tape synchronizer to begin the write operation. At status sample B time, the ON output from the block command latch sets the no transfer and correct length record latches to indicate the programming error (first storage position addressed contains group mark word mark and d-modifier in instruction is W). "Last execute cycle" ends the simulated tape write operation in the normal manner although no data transfers occurred. The processing unit then executes the next instruction in numerical sequence.

If the character in the storage position that the B-address designates is not a group mark word mark or if the d-modifier in the tape write instruction is not W, "last logic gate" of the first E-cycle resets the block command latch; the processing unit conditions "write tape call" to the tape synchronizer to begin the operation.

In an E-channel tape write operation, the processing unit executes E-cycles to transfer core storage characters to E-channel registers. The first and last E-cycles in the tape write operation process one or two useable characters from storage. All other E-cycles unload two useable characters from storage and set the characters in the result register and assembly. The result register sets E0 register; assembly sets E1 register. If the B-address is odd, the first E-cycle unloads only one useable character from storage; the character sets the E1 register; E0 register is not set. If the d-modifier is W and a group mark word mark is located in an even address storage position, the last E-cycle unloads only one useable storage character (the group mark word mark). The group mark word mark is not set in either E0 or E1 register. If the second character that the E-cycle processes to the B-channel is a group mark word mark and the d-modifier is W, the first B-channel character sets E0 register; the group mark word mark is returned to storage. When the processing unit senses the condition that the d-modifier specifies, it sets the internal end of transfer latch and conditions "disconnect call" to the tape synchronizer.

When E0 and E1 registers contain characters, E0 register sets E2 register. When E1 register contains a character and E0 register is empty, E1 register sets E2 register. The processing unit executes the next E-cycle when E0 and E1 registers are both empty if the condition to end the operation was not sensed on the previous E-cycle.

If the operation code in the tape write instruction is L (load mode), each character set in E2 register is examined to determine whether the character contains a word mark or if the character is a word separator character. If the character in the E2 register satisfies either condition, it sets the word separator latch. The

word separator latch unconditionally loads a word separator character in E3 register. When the tape synchronizer accepts the word separator character in E3 register, the character in E2 register then transfers to E3 register. For example, a word separator character from core storage causes the processing unit to transfer two word separator characters to the tape synchronizer. A normal character from core storage containing a word mark causes the processing unit to transfer a word separator character and then the normal character from storage to the tape synchronizer. If the operation code in the tape write instruction is M (move mode), the character in E2 register sets E3 register; word marks are ignored, and word separator characters from core storage are processed as normal characters.

All character transfers from E3 register to the read-write register in the tape synchronizer are under tape synchronizer control.

Characters are stored in core storage in odd parity. If the tape write instruction specifies that the tape record be written in even parity, the C-bit in the character in E3 register is inverted. When an E-cycle processes a valid blank (C-bit) from storage in even parity operation, the assembly converts the C-bit to an A-bit and gates the A-bit to E0 or E1 register. When the A-bit transfers to E3 register, a C-bit is added to the character to correct the character for even parity. Therefore, a blank from storage transfers to the tape synchronizer as an A- and C-bit.

The tape synchronizer drops "tape in process" to the E-channel when it completes read checks on the written tape record. "Not tape in process" allows the processing unit to set the external end of transfer latch. "External end of transfer" and "internal end of transfer" set the status sample B latch.

1410 E-Channel Tape Write Operation

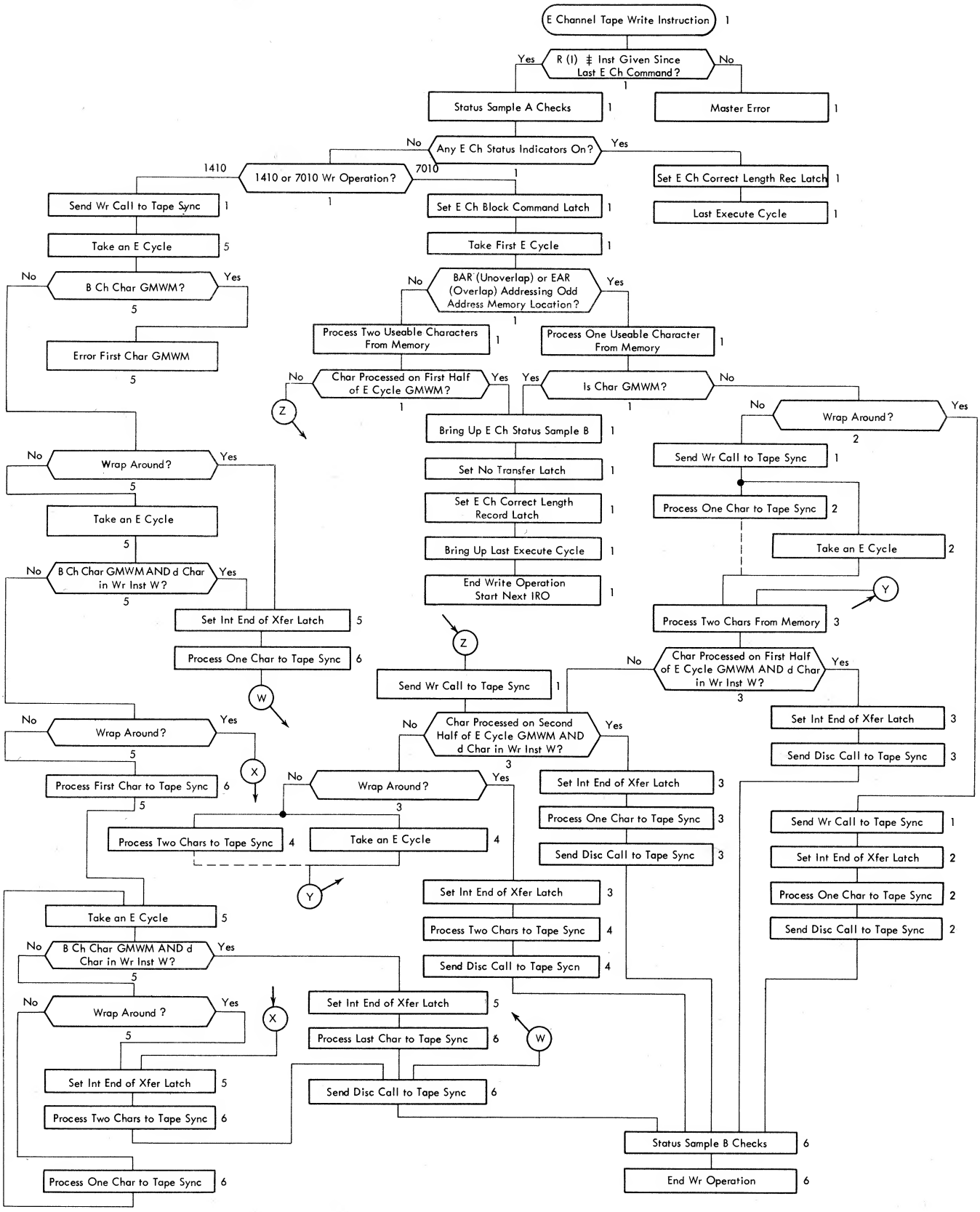
In a 1410 E-channel tape write operation, the processing unit conditions "write tape call" to the tape synchronizer at the end of status sample A time to initiate the write operation. The processing unit then executes an E-cycle to unload the character from the storage position that the B-address in the tape write instruction specifies. The character moves from storage, onto the B-channel, through assembly to the E1 register. E1 register sets E2 register. When the character in E1 register transfers to E2 register, the processing unit executes another E-cycle to unload the next character from core storage if the condition to end the tape write operation was not sensed on the previous E-cycle. The character in E2 register sets the read-write register in the tape synchronizer.

If the operation code in the tape write instruction is L, designating load mode operation, each character read from storage is examined to determine whether the character contains a word mark or if the character is the word separator character. If the character unloaded from storage satisfies either condition, it sets the E1 register word separator latch. The character is gated to E1 register but does not transfer to E2 register when E2 register is empty. Instead, the word separator latch unconditionally sets a word separator character in E2 register. When the tape synchronizer unloads the word separator character in E2 register, the character in E1 register then transfers to E2 register. For example, a word separator character from core storage causes the processing unit to transfer two word separator characters to the tape synchronizer. A character from core storage containing a word mark causes the tape synchronizer to transfer the word separator character then the character from storage to the tape synchronizer. If the operation code in the tape write instruction is M, designating move mode operation, only the character in E1 register sets E2 register; word marks in storage are ignored, and word separator characters in storage are processed as normal characters.

All character transfers from E2 register to the read-write register in the tape synchronizer are under tape synchronizer control.

When the processing unit senses the condition that the d-modifier in the write instruction specifies to end the operation, the processor sets the internal end of transfer latch and transmits "disconnect call" to the tape synchronizer. When the tape synchronizer completes read checks on the written tape record, it drops "tape in process" to the E-channel. "Not tape in process" and "internal end of transfer" set the status sample B trigger.

Characters are stored in core storage in odd parity. If the tape write instruction specifies that the tape record be written in even parity, the C-bit in the character in E2 register is inverted when the character transfers from E2 register to the E-channel. When an E-cycle processes a valid blank (C-bit) from storage in even parity operation, the assembly converts the C-bit and gates the A-bit to E1 register. When the A-bit transfers from E2 to the E-channel, a C-bit is added to the character to correct the character for even parity. Therefore, a blank from storage transfers to the tape synchronizer as an A-bit and C-bit.



* Numbers beside blocks indicate the sheet of the E Channel Tape Write Operation Flow Chart (Figure 14) that shows detail of the action.

Figure 13. Simplified E-Channel Tape Write Operation

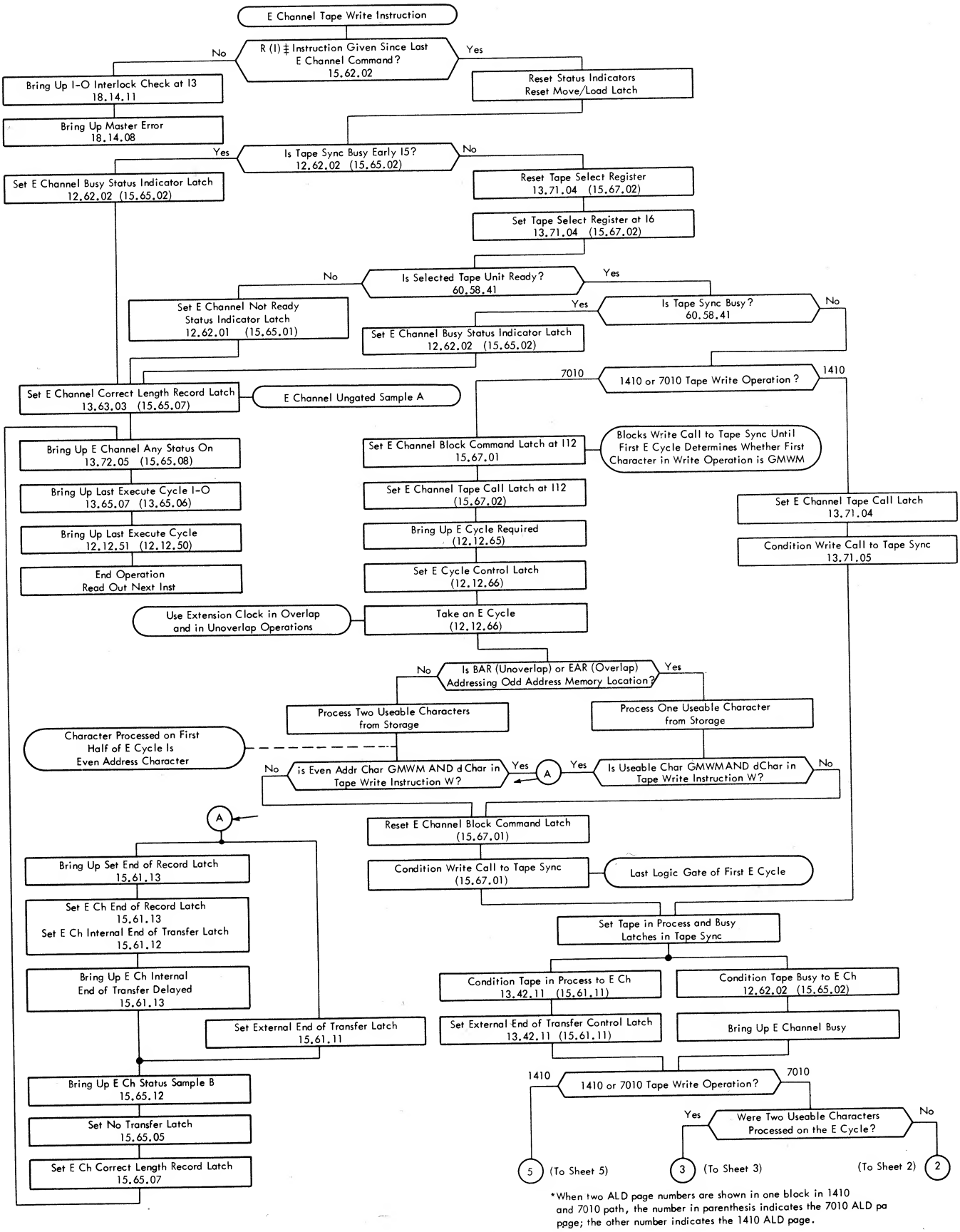


Figure 14. E-Channel Tape Write Operation (Sheet 1 of 6)

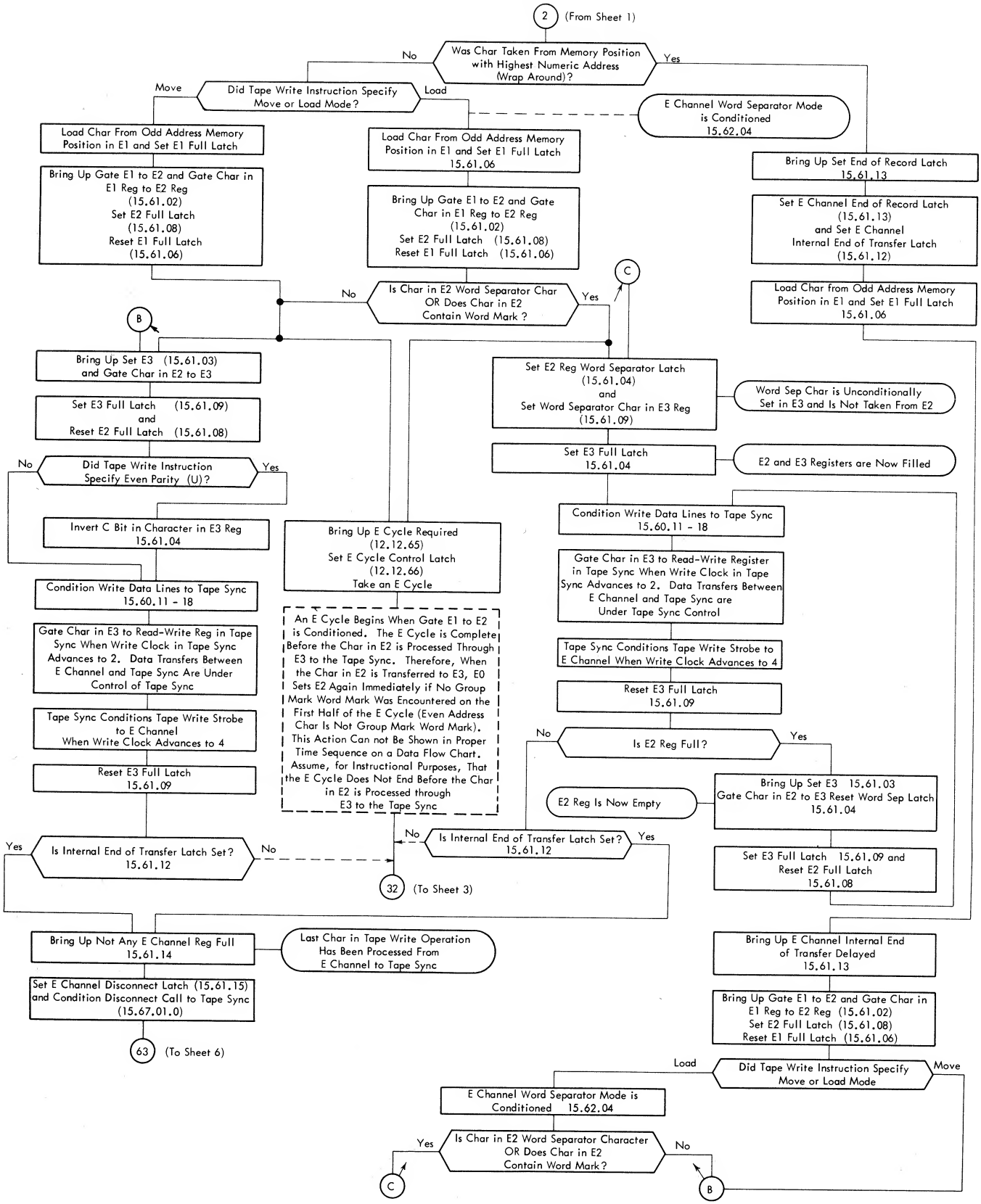


Figure 14. E-Channel Tape Write Operation (Sheet 2 of 6)

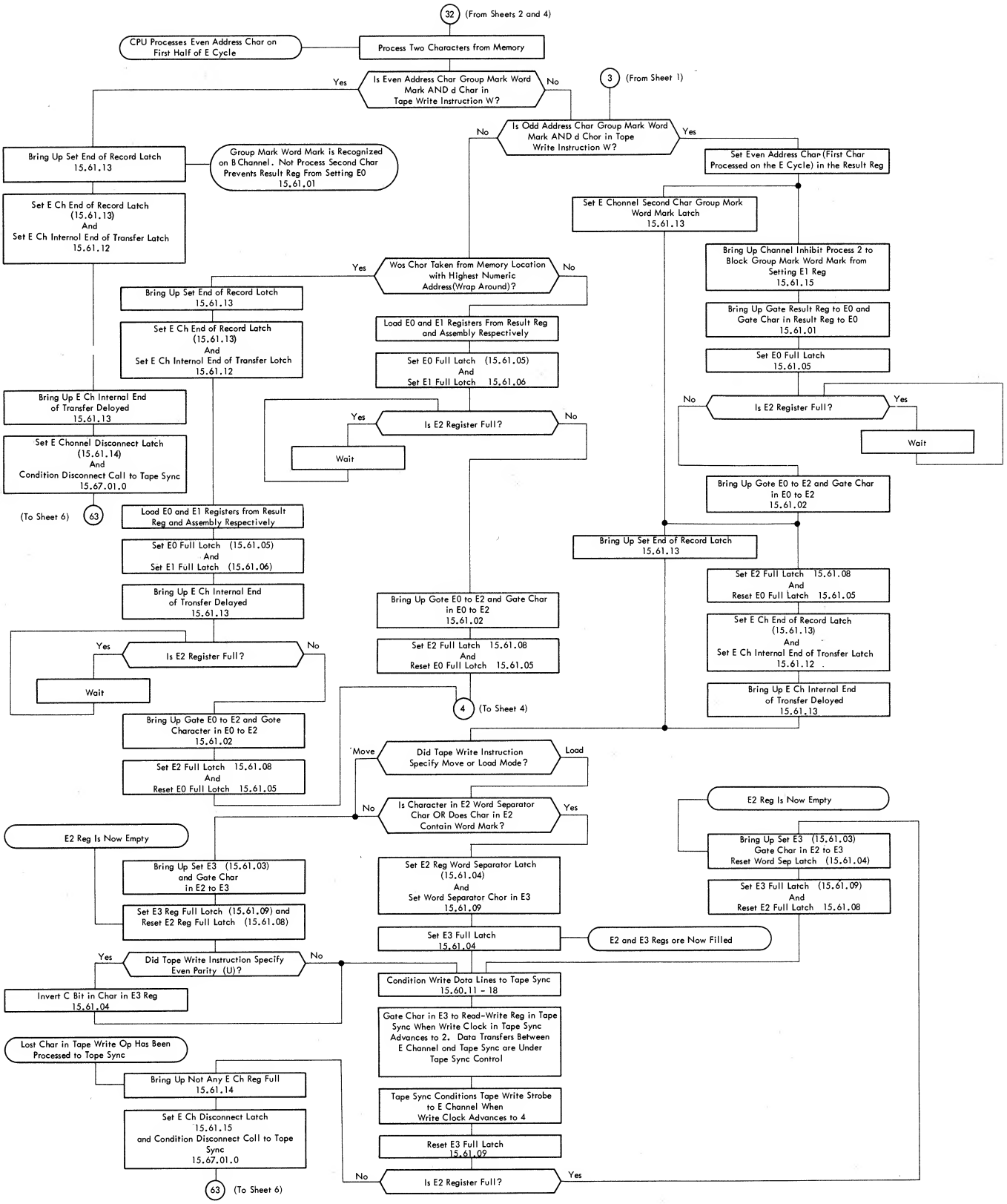


Figure 14. E-Channel Tape Write Operation (Sheet 3 of 6)

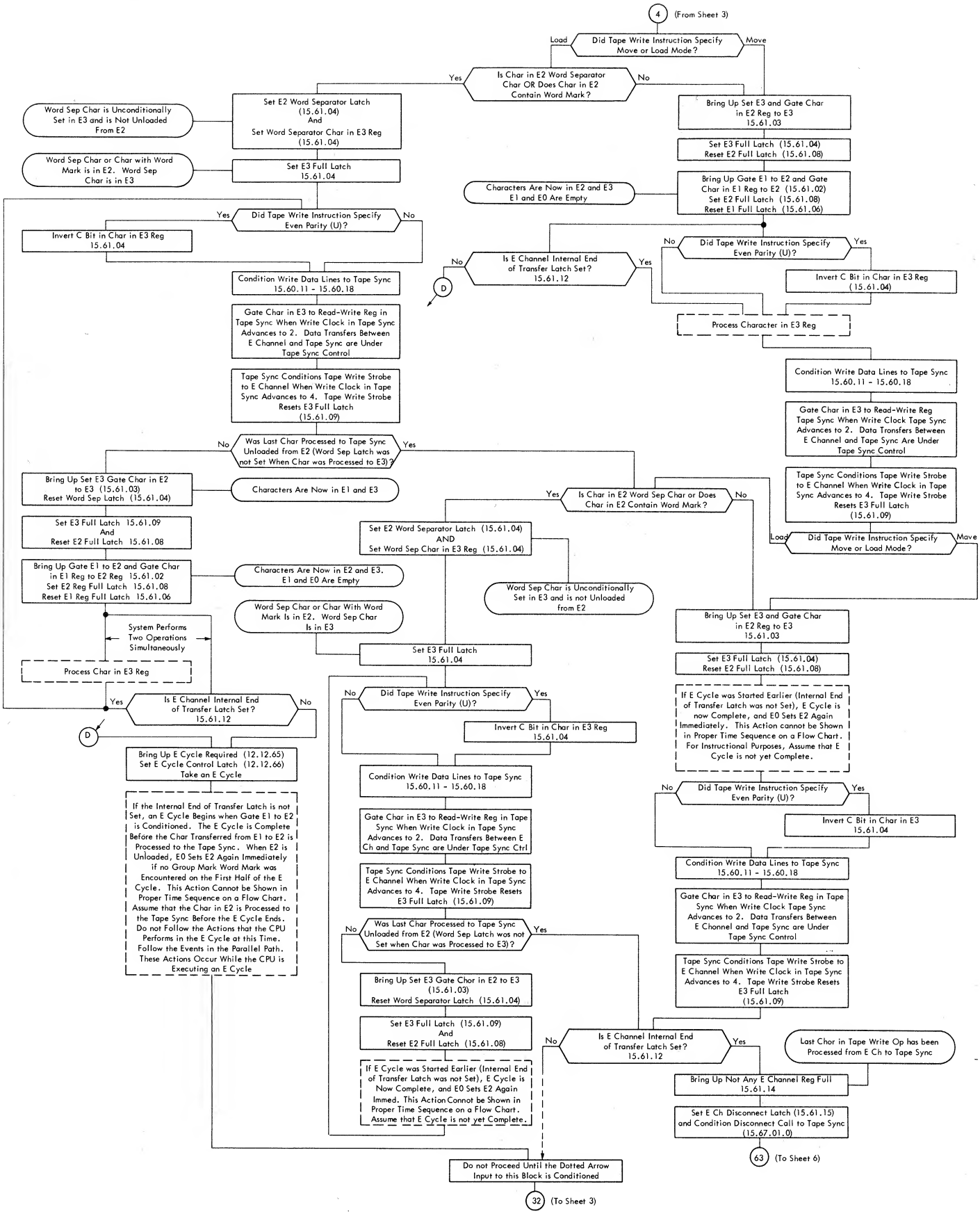


Figure 14. E-Channel Tape Write Operation (Sheet 4 of 6)

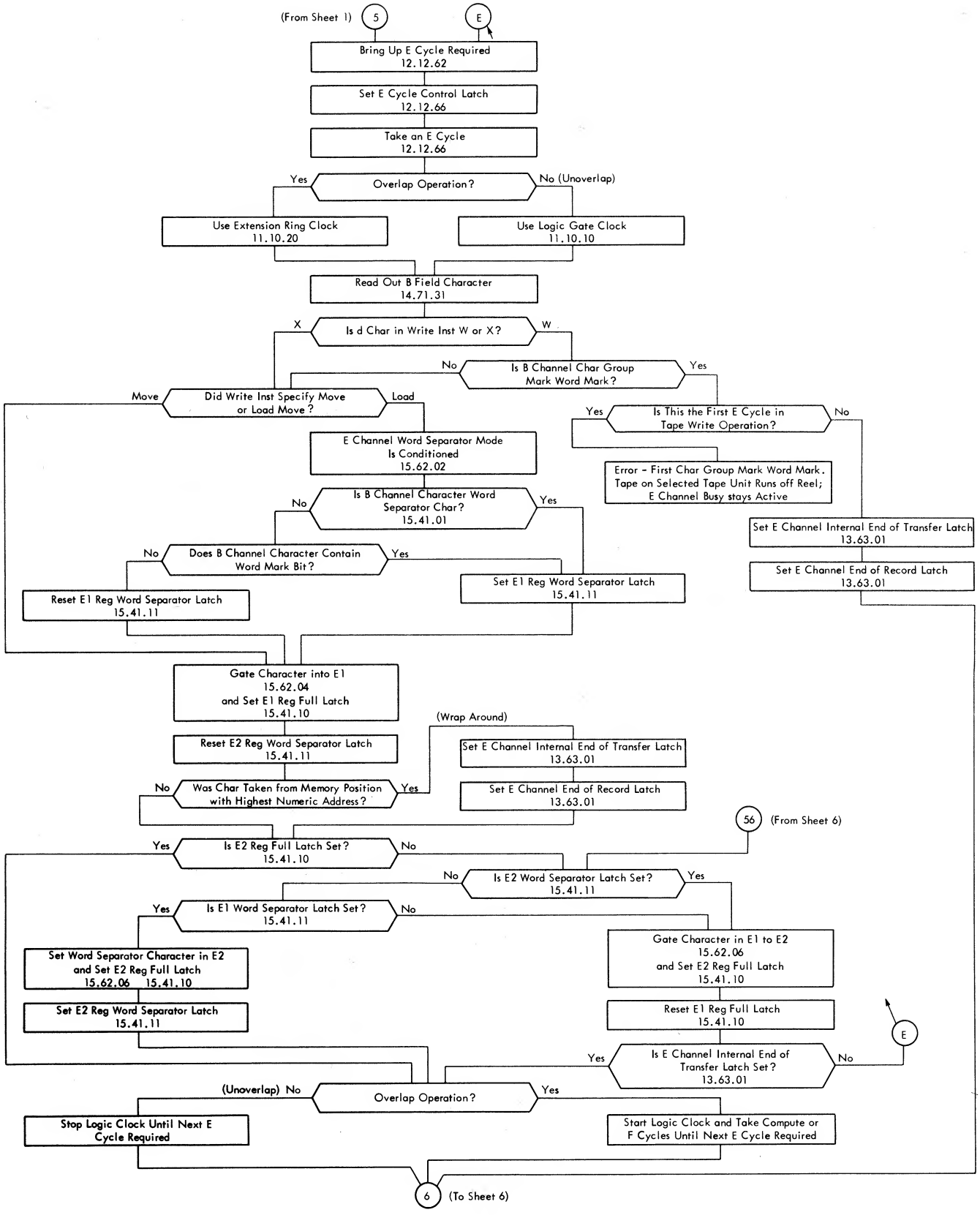


Figure 14. E-Channel Tape Write Operation (Sheet 5 of 6)

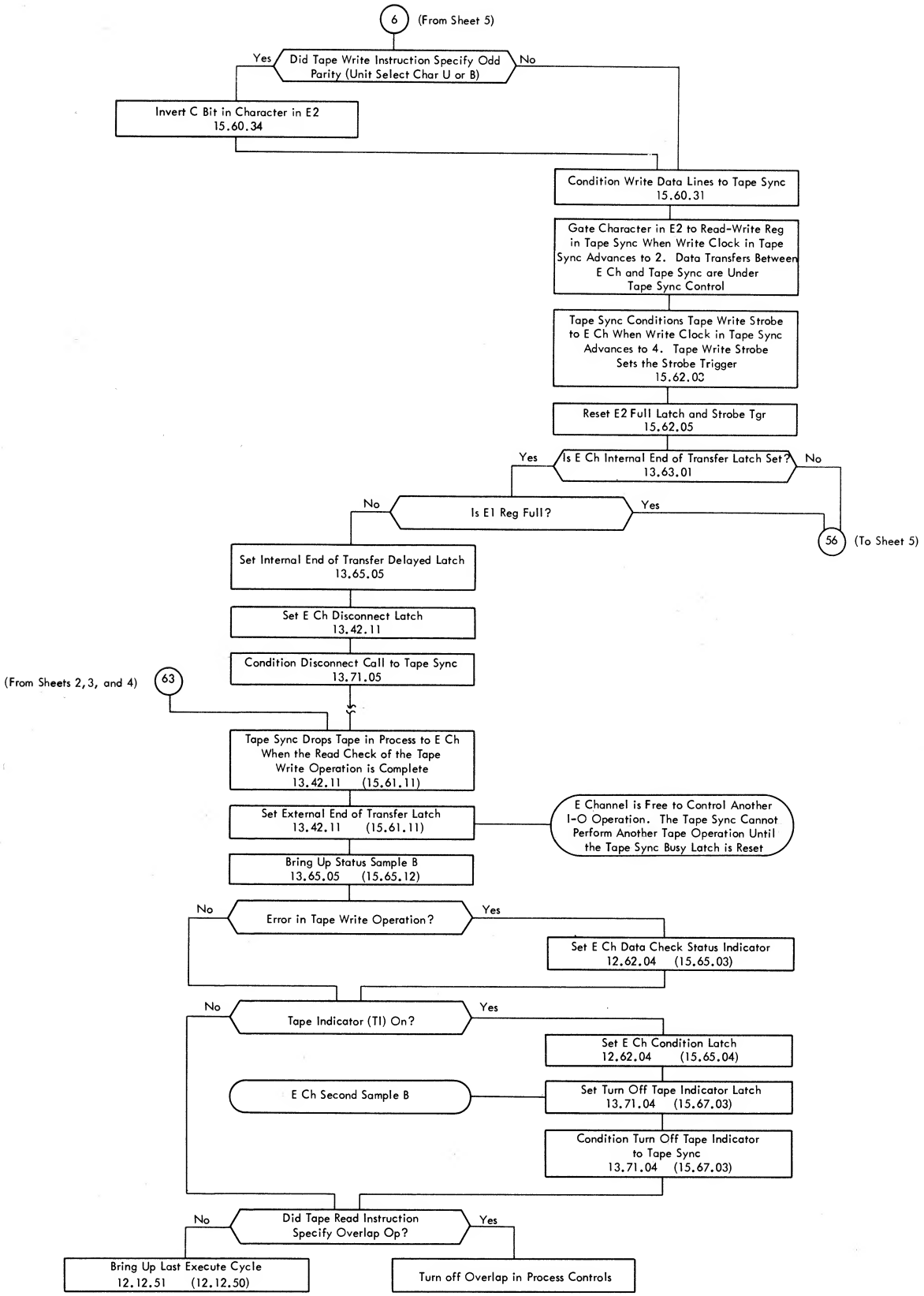


Figure 14. E-Channel Tape Write Operation (Sheet 6 of 6)

Channel Tape Read Operations

In a tape read operation, the processing unit conditions "tape read call" to the tape synchronizer at the end of status sample A time to initiate the read operation. The selected tape unit reads data from magnetic tape and transfers characters to the tape synchronizer. Each data character from the tape unit is gated to the read-write register in the tape synchronizer. The tape synchronizer gates the read-write register character onto the channel input data lines and transmits "tape read strobe" to the processing unit. "Tape read strobe" gates the tape character into the channel's E1 or F1 register on the 1410 system or E2, F2, G2, or H2 register on the 7010 system.

The processing unit stores characters in core storage in odd parity. If the tape read instruction specifies that the tape unit read the record in even parity:

1. C-bits in characters in E3, F3, G3, or H3 register are inverted in 7010 operation.

2. C-bits in the even parity characters from the tape synchronizer are inverted when the characters transfer to E1 or F1 register in 1410 operation.

When an even parity tape record contains the character with the bit structure A- and C-bits, the processing unit inverts the C-bit to change the character to odd parity, leaving only the A-bit. Because the tape instruction specified that the tape record be read in even parity, this special A-bit character is converted to a C-bit character (blank) before the processing unit loads the character in core storage. For this reason, the character with the bit structure A-bit in core storage should not be written on tape in even parity; when the record is read, the character is transferred to storage as a blank (C-bit). The A-bit to C-bit conversion occurs only in even parity operation when the tape synchronizer transfers the character with the bit structure A- and C-bits.

Tape mark characters detected in the read operation are transferred to the processing unit and handled as normal characters. Because the bit configuration of the tape mark character is always even, tape marks should be written and read from tape only in even parity operations. In odd parity operation, parity correction circuits do not alter the parity of characters transferred from the tape synchronizer. When a tape mark or any other even parity character transfers to the processing unit in odd parity operation, the asterisk insert switch must be on to:

1. Block the conditioning of the "master error" line, allowing the processing unit to continue the operation.
2. Write an asterisk in the designated core storage location in place of the invalid even parity character.

The processing unit sets the internal end of transfer latch when it detects the condition that the d-modifier in the tape read instruction specifies. The processing unit does not execute E-cycles after the internal end of transfer latch is set.

If the d-modifier in the tape read instruction is R, the processing unit sets the internal end of transfer latch when an E-cycle detects a group mark word mark from storage or senses the end of storage indication. If the d-modifier in the tape read instruction is $ and the operation is executed in unoverlap mode, the processing unit handles group mark word marks in storage as normal characters. Only the end of storage indication or a tape record too short to fill the reserved memory positions causes the processing unit to set the internal end of transfer latch. The processing unit must store the last character in the tape record in the memory location with the highest numeric address to prevent setting the wrong length record latch. If the tape read instruction with the $ d-modifier specifies overlap operation, the processing unit executes the instruction as if the $ d-modifier were R. A group mark word mark in storage or the end of storage indication causes the processing unit to set the internal end of transfer latch.

The E- and F-channels on the 1410 system process characters from the tape synchronizer to core storage in the same manner. The 7010 E-, F-, G-, and H-channel actions in the tape read operation are alike. Figure 15 shows diagrammed channel actions in a tape read operation.

7010 E-Channel Tape Read Operation

If the operation code in the tape read instruction is L (load mode), the processing unit examines the bit structure of each input character. A word separator character (1-, 4-, 8-, A-, and C-bits) in E2 register sets the word separator latch; the character does not transfer to E3 register. The next character from the tape synchronizer sets E2 register. If the character is another word separator character and the word separator latch is set, the word separator character in E2 register transfers to E3 register; the word separator latch is reset. If the character is not a word separator character and the word separator latch is set, a word mark is added to the character; the character and the word mark transfer to E3 register, and the word separator latch is reset. Two successive word separator characters from the tape synchronizer are processed to E3 register as a single word separator character in load mode operation. A word separator character followed

by the character T from the tape synchronizer transfer to E3 register as the character T with a word mark ($\check{T}$) in load mode operation.

If the operation code in the tape read instruction is M (move mode), the processing unit stores each character received from the tape synchronizer before the condition to end the operation is detected; word separator characters are processed as normal characters. The word separator latch is not set in move mode operation. In either move or load mode operation, the processing unit sets E3 register with a character from E2 register.

The character in E3 register transfers to E0 register or to E1 register. If the B-address in the tape read instruction is odd, the first character set in E3 register in the read operation transfers to E1 register. In all other cases, the character in E3 register transfers to:

1. E0 register if both E0 and E1 registers are empty.
2. E1 register only if E0 register contains a character.

The processing unit executes an E-cycle when either:

1. A character transfers from E3 register to E1 register and the condition to end the operation has not been detected, or
2. The tape synchronizer drops "tape in process", signalling the end of the tape record before the processing unit sets the internal end of transfer latch.

In searching for a group mark word mark in storage, an odd B-address causes the first E-cycle to unload from storage and process to the B-channel only one character that can affect the read operation. In all other cases, E-cycles in the read operation process two useable characters from storage to the B-channel.

If the first useable character that the E-cycle gates to the B-channel is a group mark word mark and the d-modifier is R, the processing unit sets the internal end of transfer latch and returns the characters to storage. If a character is left in either E0 or E1 register at the end of the E-cycle, indicating that the tape record is longer than the number of storage positions reserved for tape data, the processing unit sets the wrong length record condition latch.

If the second useable character that the E-cycle gates to the B-channel is a group mark word mark and the d-modifier is R, the processing unit sets the internal end of transfer latch, loads the character in E0 register and the group mark in storage. If a character is left in E1 register at the end of the E-cycle, the processing unit sets the wrong length record condition latch.

If neither of the useable characters that the E-cycle gates to the B-channel is a group mark word mark or if the d-modifier in the tape read instruction is not R, the processing unit loads the characters in E0 and E1 registers in the result register and assembly respectively. The result register and assembly gate the characters to the storage positions unloaded earlier in the E-cycle. The E-channel then waits for the tape synchronizer to transfer the next character to E2 register.

The processing unit does not execute E-cycles after the internal end of transfer latch is set. The tape synchronizer continues to condition data lines and "tape read strobe" to the processing unit until the selected tape unit reads the complete record. The E-channel is committed to the read operation and cannot perform status sample B checks until the processing unit sets the internal end of transfer latch *and* the tape synchronizer drops "tape in process." "Not tape in process" allows the processing unit to set the external end of transfer latch.

If the tape synchronizer allows the external end of transfer latch to turn on before the processing unit sets the internal end of transfer latch, "external end of transfer" forces the last E-cycle in the operation. Tape synchronizer timings allow this condition to occur only when E0 and E1 registers are both empty or when E0 register contains a character and E1 register is empty. If the first character that the forced E-cycle gates to the B-channel is a group mark word mark and the d-modifier is R, the processing unit sets the internal end of transfer latch and returns both characters to storage; a character left in E0 register at the end of the E-cycle blocks the set path to the end of record latch; "not end of record" is active at status sample B time. If the second character that the forced E-cycle gates to the B-channel is a group mark word mark and the d-modifier is R, the processing unit sets the internal end of transfer latch and:

1. If a character is in E0 register, loads the E0 register character and the group mark word mark in storage and sets the end of record latch.
2. If E0 register is empty, returns both characters read out of storage to their memory positions. Because the tape record is not long enough to fill all positions reserved in storage for tape data, the processing unit sets the wrong length record condition latch.

If neither character gated to the B-channel is a group mark word mark and the end of storage indication is not sensed, the processing unit sets the internal end of transfer latch, but does not set the end of record latch. If a character is in E0 register, the E-cycle loads memory with the character in E0 register and the second character gated to the B-channel. If E0 register is empty, both characters unloaded from memory are returned to their memory positions.

"External end of transfer" and "internal end of transfer" set the status sample B latch. If either the wrong

length record condition latch is set or the end of record latch is not set at status sample B time, the processing unit turns on the wrong length record latch.

1410 E-Channel Tape Read Operation

If the operation code in the tape read instruction is L (load mode), the processing unit examines the bit structure of each input character. A word separator character (1-, 4-, 8-, A-, and C-bits) in E1 register causes the processing unit to set the E1 and E2 word separator latches; the character is lost. The next character from the tape synchronizer sets E1 register. If the character is another word separator, the ON outputs from E1 and E2 word separator latches allow the word separator to transfer to E2 register as a normal character. If the character is not a word separator, E1 word separator latch is reset; because E2 word separator latch is set, the C- and word mark-bits in the character are inverted. The character with a word mark transfers to E2 register. The E2 word separator latch is reset during the E-cycle that gates the E2 character to storage. Two successive word separator characters from the tape synchronizer are processed to E2 register as a single word separator character in load mode operation. A word separator character followed by the character T from the tape synchronizer transfers to E2 register as the character T with a word mark (T) in load mode operation. If the operation code in the tape read instruction is M (move mode), the processing unit stores each character received from the tape synchronizer before the condition to end the operation is detected; word separator characters are processed as normal characters. Neither E1 nor E2 word separator latches are set in move mode operation. In either move or load mode operation, a character from the tape synchronizer sets E1 register. E2 register is loaded with a character from E1 register.

The processing unit executes an E-cycle when either:

1. A character transfers from E1 register to E2 register and the condition to end the operation has not been detected, or
2. The tape synchronizer drops "tape in process," signalling the end of the tape record, before the processing unit sets the internal end of transfer latch.

In searching for the condition that the d-modifier in the read instruction specified to end the operation, the first E-cycle unloads the character in the memory position designated by the B-address register (unoverlap) or E-address register (overlap). The following E-cycles unload characters from the next sequentially higher memory positions. Characters that E-cycles process from storage move onto the B-channel.

If the B-channel character is a group mark word mark and the d-modifier in the read instruction is R, the processing unit sets the internal end of transfer latch and returns the group mark word mark to storage; the character in E2 register is not gated to storage. Because the tape record is longer than the number of memory positions reserved for tape data, the processing unit sets the wrong length record latch at status sample B time.

If the B-channel character is not a group mark word mark or the d-modifier in the read instruction is not R, the processing unit gates the character in E2 register to the storage location unloaded earlier in the E-cycle. The E-channel then waits for the tape synchronizer to transfer the next character to E1 register.

The processing unit does not execute E-cycles after the internal end of transfer latch is set. The tape synchronizer continues to condition data lines and "tape read strobe" to the processing unit until the selected tape unit reads the complete record. The E-channel is committed to the tape read operation and cannot perform status sample B checks until the processing unit sets the internal end of transfer latch AND the tape synchronizer drops "tape in process". "Not tape in process" allows the processing unit to set the external end of transfer latch.

If the tape synchronizer allows the external end of transfer latch to turn on before the processing unit sets the internal end of transfer latch, "external end of transfer" forces the last E-cycle in the operation. Tape synchronizer timings allow this condition to occur only when the E2 register is empty. If the character that the forced E-cycle gates to the B-channel is a group mark word mark and the d-modifier in the read instruction is R, the processing unit sets the internal end of transfer latch and returns the group mark word mark to storage. Because no character is in E2 register, the processing unit does not set the wrong length record latch at status sample B time.

If the character that the forced E-cycle gates to the B-channel is not a group mark word mark, the processing unit returns the character to storage and sets the internal end of transfer latch; the end of record latch is not set.

"Internal end of transfer" and "external end of transfer" set the status sample B trigger. If either E2 register contains a character or the end of record latch is not set at status sample B time, the processing unit sets the wrong length record latch.

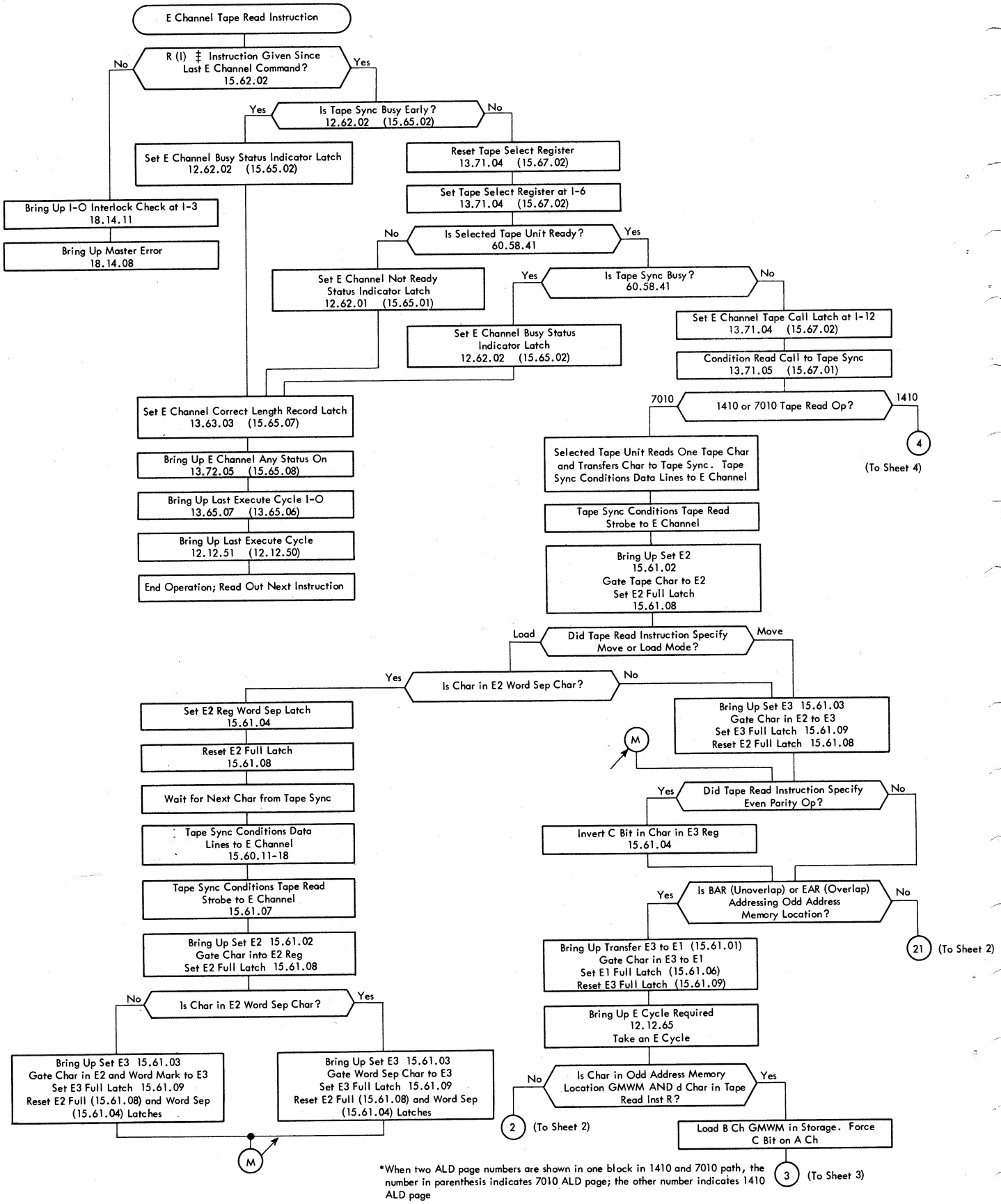


Figure 15. E-Channel Tape Read Operation (Sheet 1 of 5)

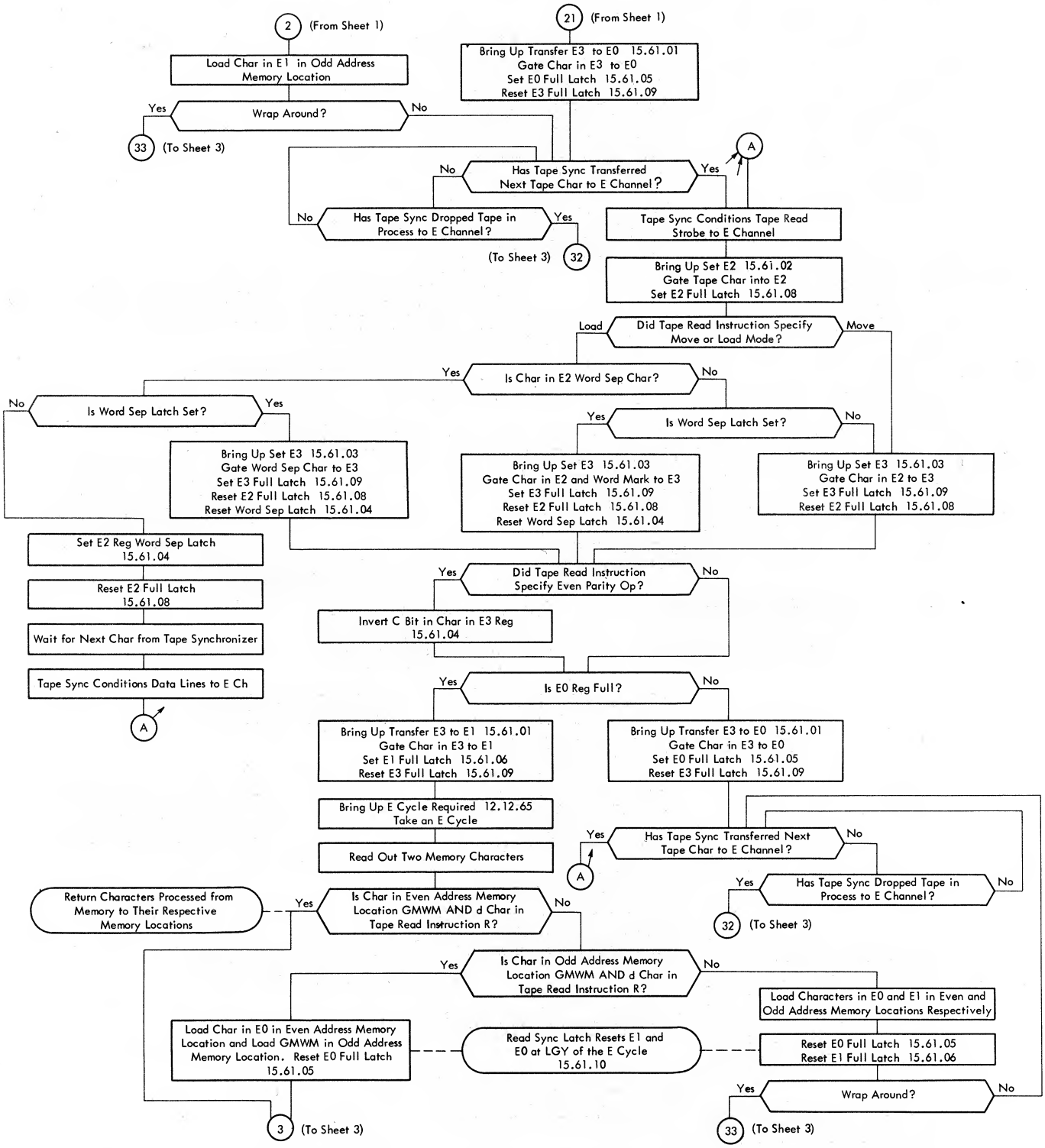


Figure 15. E-Channel Tape Read Operation (Sheet 2 of 5)

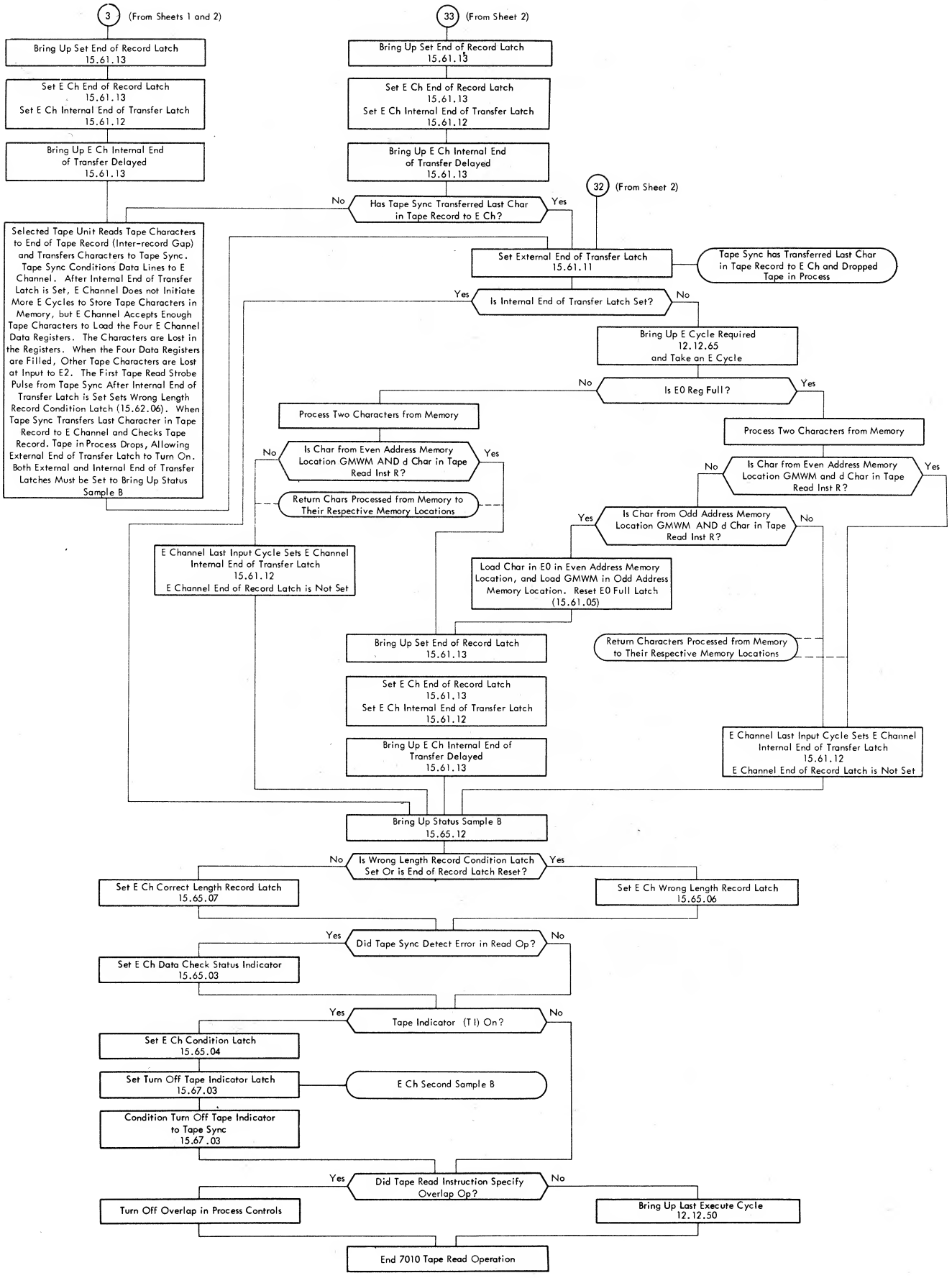


Figure 15. E-Channel Tape Read Operation (Sheet 3 of 5)

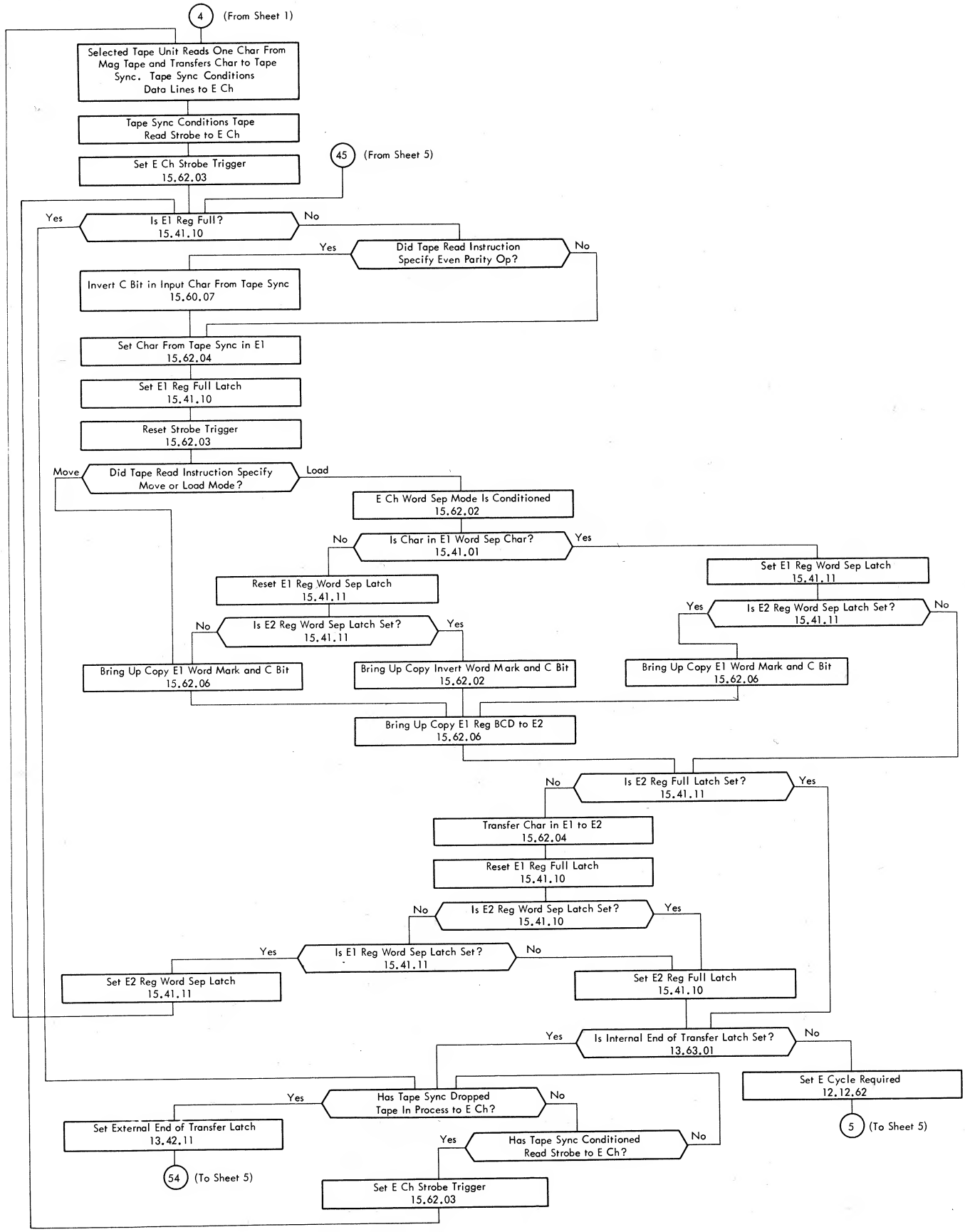


Figure 15. E-Channel Tape Read Operation (Sheet 4 of 5)

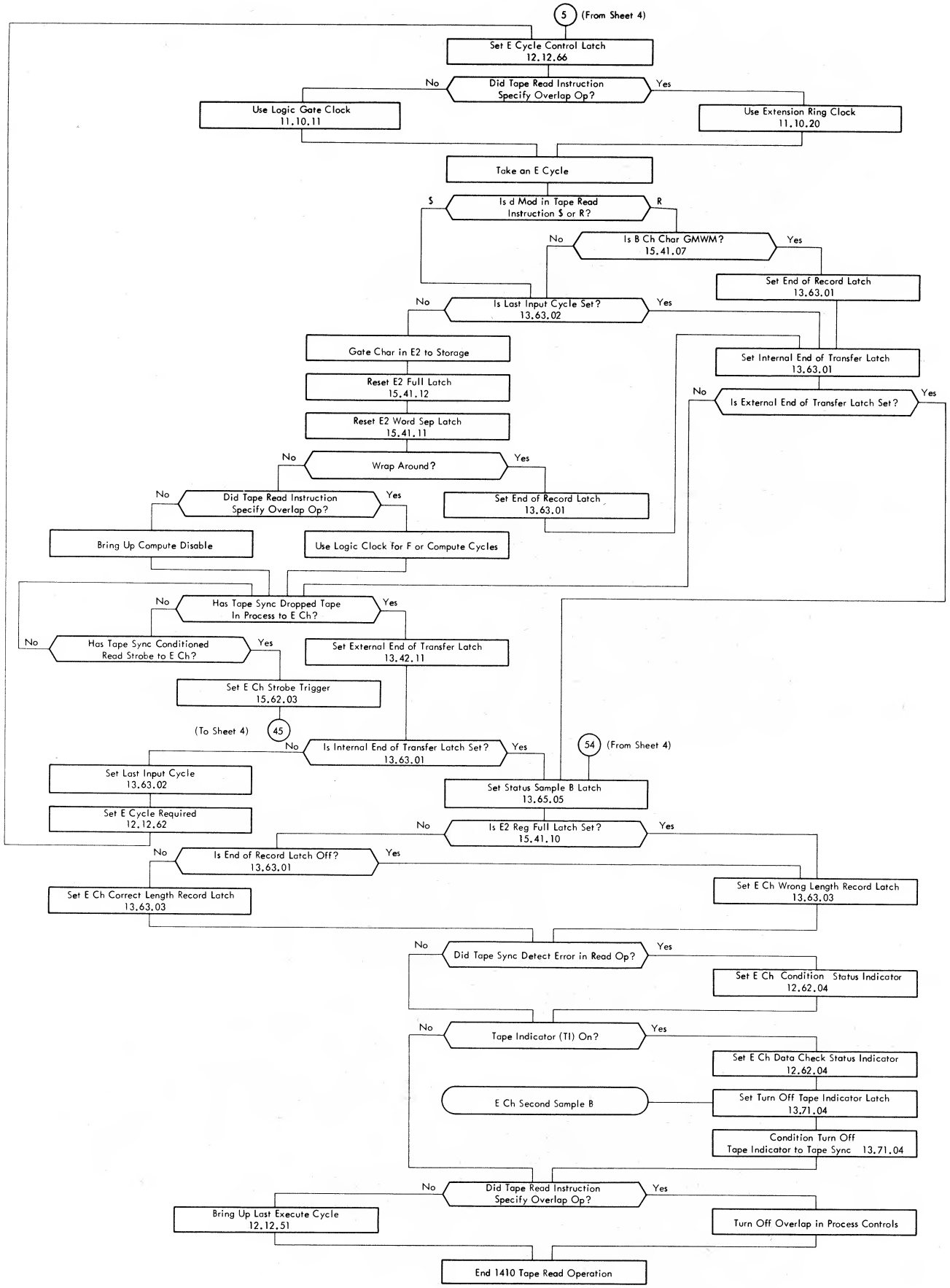


Figure 15. E-Channel Tape Read Operation (Sheet 5 of 5)

Channel Tape Unit Control Operation

The tape unit control instruction specifies one of five tape operations: write tape mark, backspace, rewind, rewind unload, or erase. The d-modifier in the unit control instruction designates the unit control operation to be executed.

Tape unit control operations do not require data transfers between the processing unit and the tape synchronizer. The write tape mark operation is the only unit control operation that requires the selected tape unit to record a character on magnetic tape. In this case, however, the tape synchronizer automatically generates the character.

Each unit control instruction causes the selected processing unit channel to unconditionally set the corresponding correct length record latch, even if the tape unit does not execute the operation.

When the processing unit decodes a unit control instruction, it conditions "compute disable" for 25 microseconds at I-ring 6 time, stopping the clock in the processing unit. This 25-microsecond delay, called the unit control instruction read out delay, allows lines between the processing unit and the tape synchronizer to settle before the operation proceeds.

The processing unit conditions the appropriate call signal to the tape synchronizer to start the designated unit control operation if:

1. The tape synchronizer is not busy
2. The selected tape unit is in ready status
3. The unit control operation does not require the selected tape unit to move tape backward beyond load point.

In all other unit control operations except write tape mark, the processing unit has no function in the operation after sending the call signal to the tape synchronizer. The tape synchronizer and tape unit initiate and execute all subsequent actions; the processing unit channel is free to control other I-O operations. Depending on the unit control operation being performed, the tape synchronizer may or may not be designated to start another tape operation before the previous unit control operation is complete. In all cases, the tape unit must complete a tape operation before it can be selected to perform another operation.

Figure 16 shows E-channel actions in the execution of the tape unit control operations.

Write Tape Mark

When the d-modifier in the unit control instruction is M, the processing unit conditions "write tape mark call" to the tape synchronizer. "Write tape mark call" sets the tape in process, write tape mark, and disconnect latches in the tape synchronizer, initiating a one character (plus check character) write operation. The tape synchronizer returns "tape in process" and "tape busy" to the processing unit. "Tape in process" holds the channel busy line active, and blocks "external end of transfer" until the tape unit records the tape mark and check character and the tape synchronizer checks the data written on tape. The channel cannot begin another I-O operation while "tape in process" is active. "Tape busy" prevents the channel from starting another tape operation until the write tape mark operation is complete and tape synchronizer circuits reset.

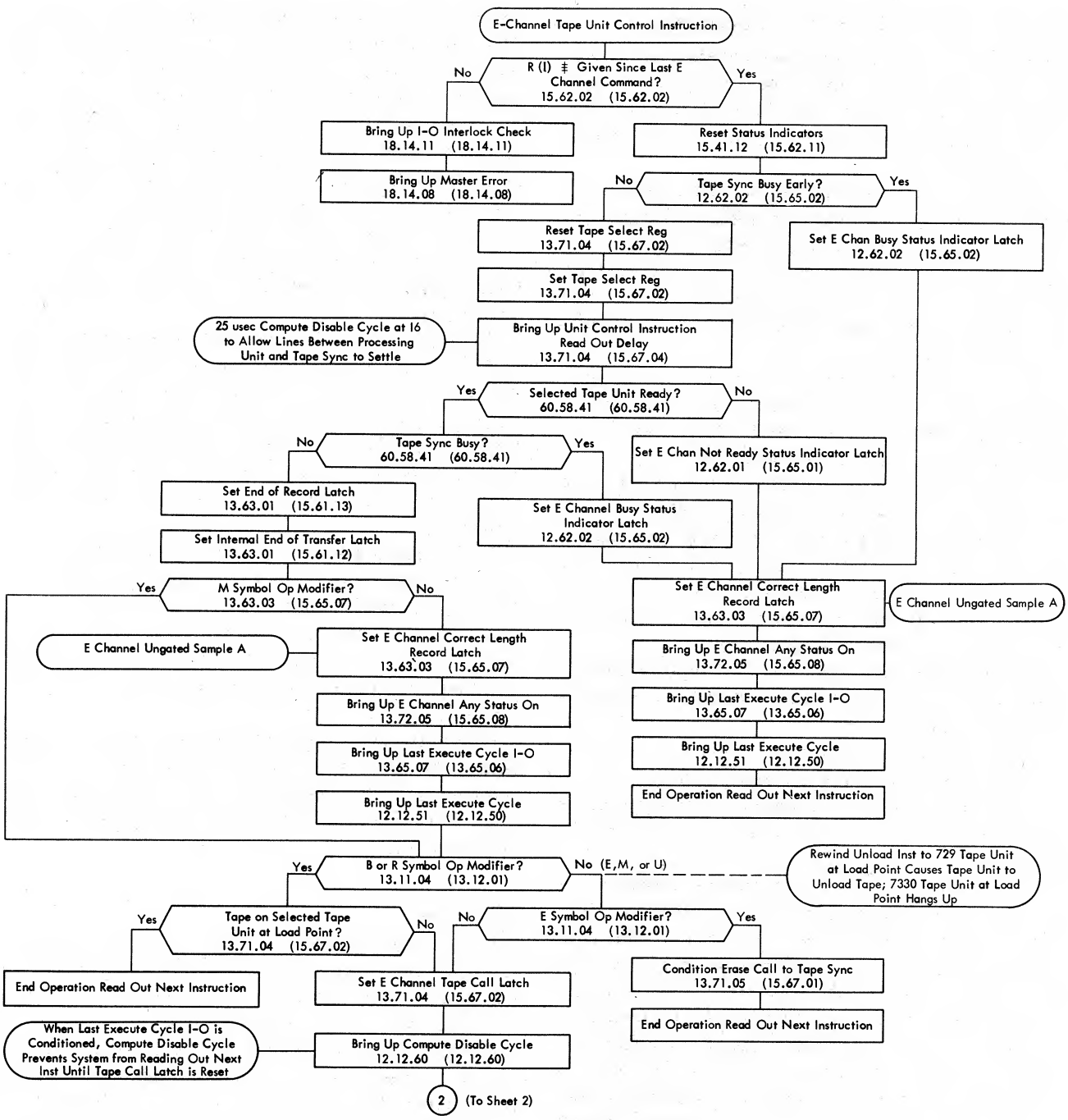
The tape synchronizer automatically conditions the 1-, 2-, 4-, and 8-bit data lines to the selected tape unit. The tape unit records the tape mark and the check character (the check character has the same bit configuration as the tape mark). The tape synchronizer cancels "tape in process" and later "tape busy" to the processing unit, ending the operation without an error if:

1. The tape mark instruction specified that the write tape mark operation be executed in even parity (U in tens position of X-control field), and
2. The tape unit recorded the tape mark without dropping an odd number of bits. A tape mark is always an even parity character and must be checked for even parity.

If the tape synchronizer detects an error while executing the write tape mark operation, it conditions "tape error" to the E-channel, causing the processing unit to set the data check status indicator at status sample B time.

Backspace

The unit control instruction with a B d-modifier causes the processing unit to condition "backspace call" to the tape synchronizer. The tape synchronizer brings up "tape busy" to the processing unit, indicating that the synchronizer is engaged in a tape operation and cannot execute another operation until backspacing is complete. The processing unit has no function in the backspace operation after transmitting "backspace call"; the tape synchronizer and the selected tape unit initiate and perform subsequent actions in the operation. The tape synchronizer performs no checks in the backspace operation, and "tape error" is not conditioned during the operation. The designated channel is not committed to the operation while the tape unit moves tape backward; therefore, the channel is free to address any other I-O device except a tape unit. Another tape operation cannot begin until backspacing is complete and the tape synchronizer cancels "tape busy."



* When two ALD page numbers are shown in one block in 1410 and 7101 path, the number in parenthesis indicates the 7010 ALD page; the other number indicates the 1410 ALD page.

Figure 16. E-Channel Tape Unit Control Operation (Sheet 1 of 2)

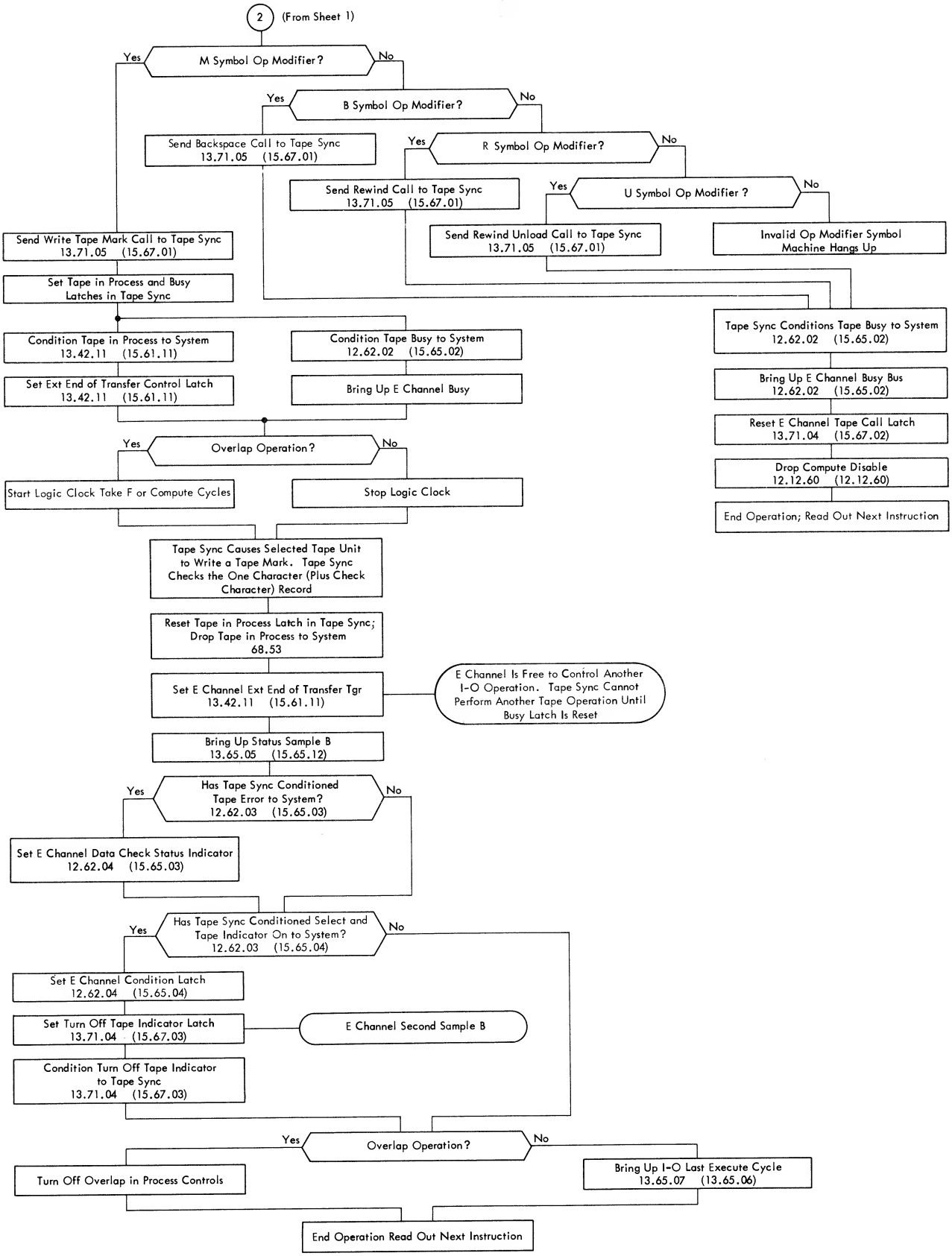


Figure 16. E-Channel Tape Unit Control Operation (Sheet 2 of 2)

If tape on the selected tape unit is at load point when the processing unit decodes the backspace instruction, the processing unit does not condition "backspace call", and the backspace operation is not executed. It is never necessary to move tape backward beyond load point.

Rewind and Rewind Unload

When the d-modifier in the unit control instruction is R (rewind) or U (rewind unload), the processing unit conditions "rewind call" or "rewind unload" to the tape synchronizer. The tape synchronizer brings up "tape busy" to the processing unit, indicating that the tape synchronizer is engaged in a tape operation and cannot execute another operation. The processing unit has no function in the rewind or rewind unload operation after transmitting "rewind call" or "rewind unload"; the channel is then free to control any other I-O device except the tape synchronizer.

When the selected tape unit first begins to rewind tape, it sends "select and rewind" to the tape synchronizer, causing the synchronizer to cancel "tape busy" and to relay the "select and rewind" signal to the processing unit. Actions that occur after the tape unit conditions "select and rewind" are under complete control of the selected tape unit.

The processing unit can select the tape synchronizer to perform another operation when "tape busy" drops, but "select and rewind" prevents the tape unit executing the rewind operation from being selected. Therefore, it is possible to have all tape units on the channel rewinding tape at the same time.

If tape on the selected tape unit is at load point when the processing unit decodes the rewind instruction, the channel does not condition "rewind call" to the tape synchronizer, and the rewind operation is not executed. If the processing unit decodes the rewind unload instruction when tape on the designated tape unit is at load point, the channel initiates the rewind unload operation. If the rewind unload instruction specifies a 729 tape unit, the tape unit unloads tape; if the rewind unload instruction specifies a 7330 tape unit, the tape unit "hangs up." In both cases, however, the tape unit does not move tape backward beyond load point.

Erase

The unit control instruction with an E d-modifier causes the processing unit to send "erase call" to the tape synchronizer. The unit select character in the erase instruction performs no function in the tape synchronizer execution of the erase operation. The erase instruction conditions the tape synchronizer to erase a section of tape when the subsequent write operation begins; no tape movement occurs, however, until the write operation starts. Because "erase call" does not cause the tape synchronizer to transfer to busy status, the processing unit is free to execute another tape or other I-O operation immediately.

The write magnetic tape instruction should follow the erase instruction. If a read or backspace operation is initiated while the tape synchronizer is conditioned to erase a section of tape, all erase conditions are reset. Another erase instruction and a write instruction must be given to blank a section of tape.

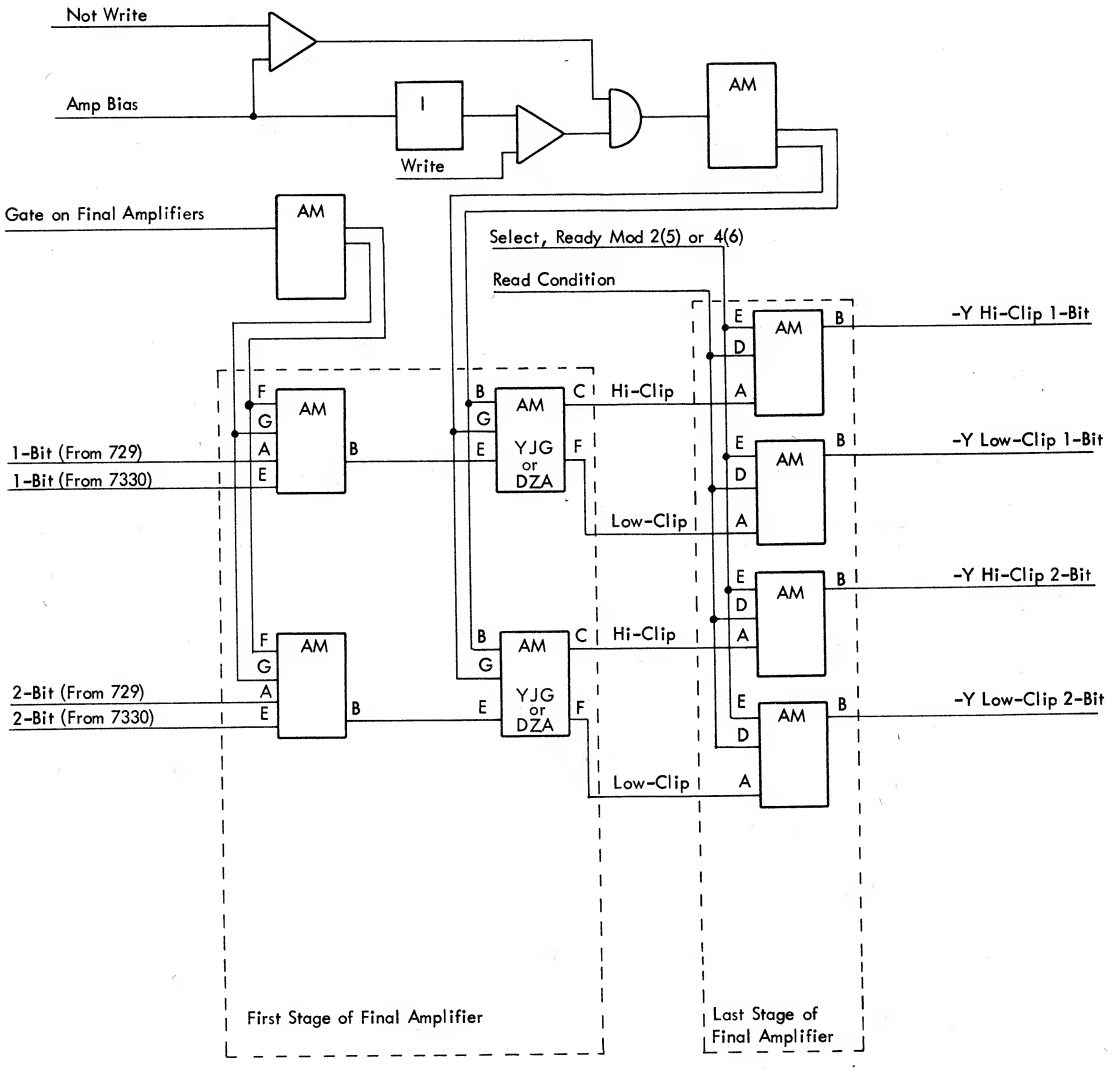
Final Amplifiers

Final amplifiers in the tape synchronizer (Figure 17) detect, filter, and amplify input data from the tape unit. Final amplifiers consist of seven identical tracks, one for each bit in the BCD code, and gating and biasing circuits. Each final amplifier track has two separately gated stages to eliminate noise transfer to the read registers.

Gating and biasing circuits establish standards for processing within the final amplifiers because:

1. Data signals from various tape units are of different frequencies.

2. Requirements that the tape synchronizer establishes for data signals in tape read operations differ from the requirements established for data pulses in tape write operations.



* only two of the seven final amplifier tracks are shown; other tracks operate in an identical manner. Final amplifiers logic is shown on system pages 60.40.10.1(1414-1 and 2) and 90.40.10.1 (1414-7)

Figure 17. Final Amplifiers

Tape Synchronizer With 800 cpi Feature**				Tape Synchronizer Without 800 cpi Feature***			
Tape Read Operation*		Tape Write Operation*		Tape Read Operation*		Tape Write Operation*	
Low-Clip Pin F	Hi-Clip Pin C	Hi-Clip Pin C	Low-Clip Pin F	Low-Clip Pin F	Hi-Clip Pin C	Hi-Clip Pin C	Low-Clip Pin F
0.00v to 0.14v	1.24v to 1.56v	1.47v to 1.93v	0.90v to 1.36v	0.00v to 0.14v	1.69v to 2.00v	2.06v to 2.50v	1.33v to 1.78v

*Chart represents values with AMP BIAS switch off; all values are positive with respect to -12v
**DZA Clipper Card
***YJG Clipper Card (1414-1 Without 800 cpi Feature)
****Values are accurate when only gates (no data pulses from tape unit) are applied to Clipper Card

Figure 18. High-Clip and Low-Clip Outputs of Final Amplifier Clipper Card

The clipping card* in each final amplifier track generates high- and low-clip outputs. The high- and low-clip pulses eliminate noise and weak data signals and produce uniform inputs to the last stage of the final amplifier track. When only gates (no data applied) to the clipper card are conditioned, levels listed in Figure 18 appear at the output of the card. Clipping levels in tape write operation are normally higher than clipping levels in a tape read operation to insure that characters written on tape are of sufficient amplitude to be read in a subsequent read operation.

When data signals of correct amplitude are applied to the clipper card, high- and low-clip outputs from the card increase to levels established by the biasing circuit. If input data signals to the clipper card are not of sufficient amplitude, one of two actions occur depending on the peak voltage of the weak signal.

1. Normal low-clip outputs might be present at the output of the clipper card, but high-clip outputs will not be affected by the data input.

2. High- or low-clip pulses may not increase with the weak data input.

For example, assume (figures for the example are selected for illustrative purposes and do not represent true voltage levels) that an 8-volt data signal at the input of the clipper card is required to yield normal high- and low-clip outputs. A 4-volt input signal will probably produce the normal low-clip output, but the high-clip output will not increase from the no data condition. A 2-volt data input will not cause a change on either the high- or low-clip output pins.

High- and low-clip outputs from the clipper cards feed the last stage of the final amplifier track. Output signals from the clipper card must rise for 5 microseconds and fall 0.2-volt to fire the Schmitt trigger at the input of the last amplifier stage. With normal inputs, high- and low-clip outputs of the last amplifier stages are approximately the same amplitude. Because 729 and 7330 tape units read and transfer characters to the tape synchronizer at different rates, the select, ready mode 2 or 4 line (conditioned when any 729 tape unit executes the tape operation) conditions the last stage of the final amplifiers to compensate for frequency differences in the input data signal.

*YJG clipper cards are used in 1414-1 tape synchronizers not equipped with the 800 cpi feature. DZA clipper cards are used in 1414-1 tape synchronizers equipped with the 800 cpi feature and in 1414-7 tape synchronizers.

Read Registers

Both read register A and read register B (Figure 19) have seven data latches, one for each bit in the BCD code. Low-clip bits from the final amplifiers set read register B data latches; high-clip bits set read register A data latches. Read register A or read register B sets the longitudinal redundancy check register (LRCR) and, in tape read operations, the read-write register.

In the read check of a tape write operation, the read registers must be loaded with a full character (due to skewgate considerations):

at read clock-4 (RC-4) time if the tape unit writing the record is recording at any other density except 800 cpi.

at read clock-5 (RC-5) time if a 729 V tape unit is performing the write operation in the 800-cpi density mode.

at read clock-6 (RC-6) time if a 729 VI tape unit is performing the write operation in the 800-cpi density mode.

In a read only operation, all bits in the character must be stored in the read registers before RC-7 time.

The tape synchronizer checks the character in read register A for a vertical redundancy error. The status of the odd redundancy latch determines whether the character is checked for odd or even redundancy. If a vertical redundancy error is detected in a tape read operation, the A register VRC latch is set, causing the A register VRC error indicator to turn on; the read-

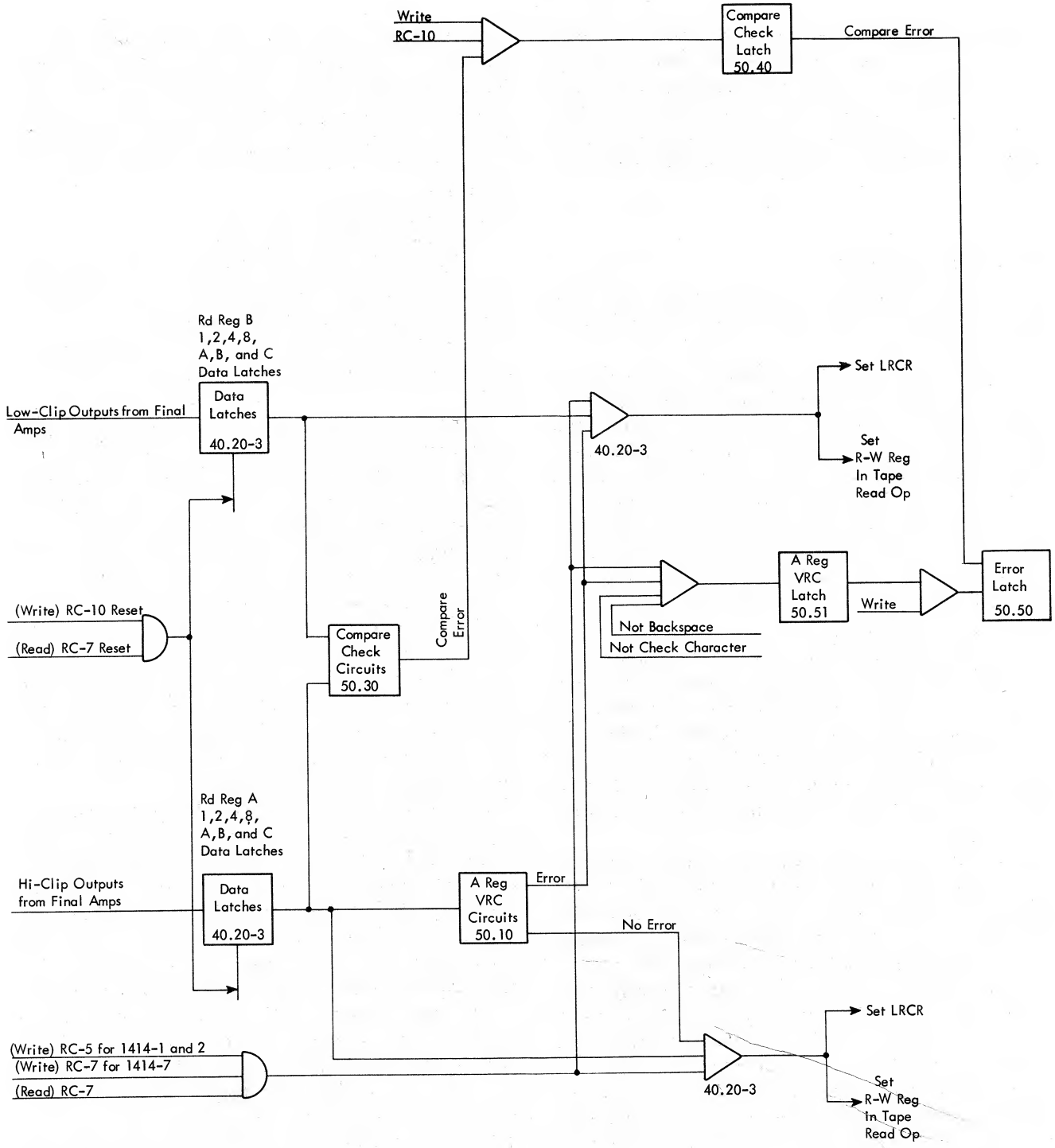


Figure 19. Read Registers

write register and the longitudinal redundancy check register (LRCR) are unconditionally loaded with the character in read register B. In a read check of a write operation, the read-write register is not loaded with a character from either read register; a vertical redundancy error in read register A sets the A register VRC and error latches, causing the A register VRC error and error indicators to turn on; read register B unconditionally sets the LRCR. If no error is detected in the character in read register A, the output of read register B is blocked, and read register A sets the LRCR and, in a tape read operation, the read-write register.

Because different final amplifier circuits set read register A and read register B, the same character might not be stored in both read registers. In the read check of a write operation, the character in read register A is compared to the character in read register B. Data in both registers should represent the same character.

Read-Write Register

The seven data latches that make up the read-write register (Figure 20) process output data from the tape synchronizer.

In a tape read operation, characters from the selected tape unit set the read registers; read register A or read register B loads the read-write register. Data stored in the read-write register are transferred to the system (processing unit 1410/7010 or data channel 7040/7044). If the system does not accept the character before the read-write register is reset, the character is lost, but the tape read operation is not interrupted. The next character from the read register sets the read-write register, and output data lines to the system are conditioned.

In a tape write operation, write clock outputs reset the read-write register and gate characters from the system to the read-write register; data are transferred to the selected tape unit to be recorded. In the read check of the tape write operation, the input to the read-write register from the read registers is blocked; read register characters cannot be loaded in the read-write register.

In a write tape mark (write end of file) operation, "write tape mark" blocks normal input paths to the read-write register and directly sets the read-write register's 1-, 2-, 4-, and 8-bit data latches, conditioning the corresponding data lines to the tape unit.

Each character loaded in the read-write register is checked for a vertical redundancy error. The status of the odd redundancy latch determines whether the character is checked for odd or even redundancy. A vertical redundancy error sets the read-write register VRC and error latches, but the tape synchronizer does not interrupt the operation if the Stop On Error CE switch is not on.

Longitudinal Redundancy Check Register (LRCR)

The seven binary triggers that make up the LRCR determine the horizontal bit structure of a record.

All LRCR triggers are set at the beginning of a tape write, read, or write tape mark operation. A delay counter output examines the status of the LRCR triggers during the write or read delay. The ON output of any LRCR trigger sets the error latch, and if all LRCR triggers are on, indicating correct LRCR operation, the gate for the first stage of the final amplifiers is conditioned. A delay counter output later in the write or read delay resets the LRCR triggers and all tape synchronizer error latches. If at least one, but not all LRCR triggers are not set:

1. No LRCR triggers are reset.
2. The error latch is not reset.
3. The gate for the first stage of the final amplifiers is not conditioned, consequently, data from tape are not processed through the final amplifiers.
4. The tape runs off the file reel in read operations and in write operations not executed on a 729 tape unit.

Input bits to the LRCR set or reset corresponding LRCR triggers to their opposite states (the first bit turns on the corresponding trigger; the second bit resets the trigger; the third bit sets the trigger, etc.). After the tape synchronizer processes the check character, all LRCR triggers should be reset; any LRCR trigger on at the end of the operation sets the error latch.

Figure 21 illustrates the LRCR action on a simple tape record containing the characters I, B, and M. Each character is checked for vertical and longitudinal redundancy errors. Assume that the system has called for even parity operation. The horizontal and vertical bit counts are even. When the tape synchronizer processes the character, all LRCR triggers are reset, indicating correct operation.

The dotted circles note bits dropped during the read check operation. The bits were written on tape, as indicated by the check character bit configuration, but were dropped during the read check of the write operation. Dotted lines represent error conditions in the sequence chart. When "LRCR sample" is active, two LRCR triggers are on, and the tape synchronizer indicates an LRCR error. Because both dropped bits are in the same character (B), the vertical structure of the character is still even, and no vertical redundancy error is registered. If only one bit had been dropped in the character, vertical and longitudinal redundancy errors would have been registered.

The tape synchronizer samples the LRCR after the check character has been read to insure that all characters are entered.

Odd-Even Character Counter

The odd-even character counter determines whether the tape record has an odd or even number of characters preceding the check character. If the character counter indicates an even number of normal characters, the odd redundancy latch is unconditionally reset, and the check character is checked for even

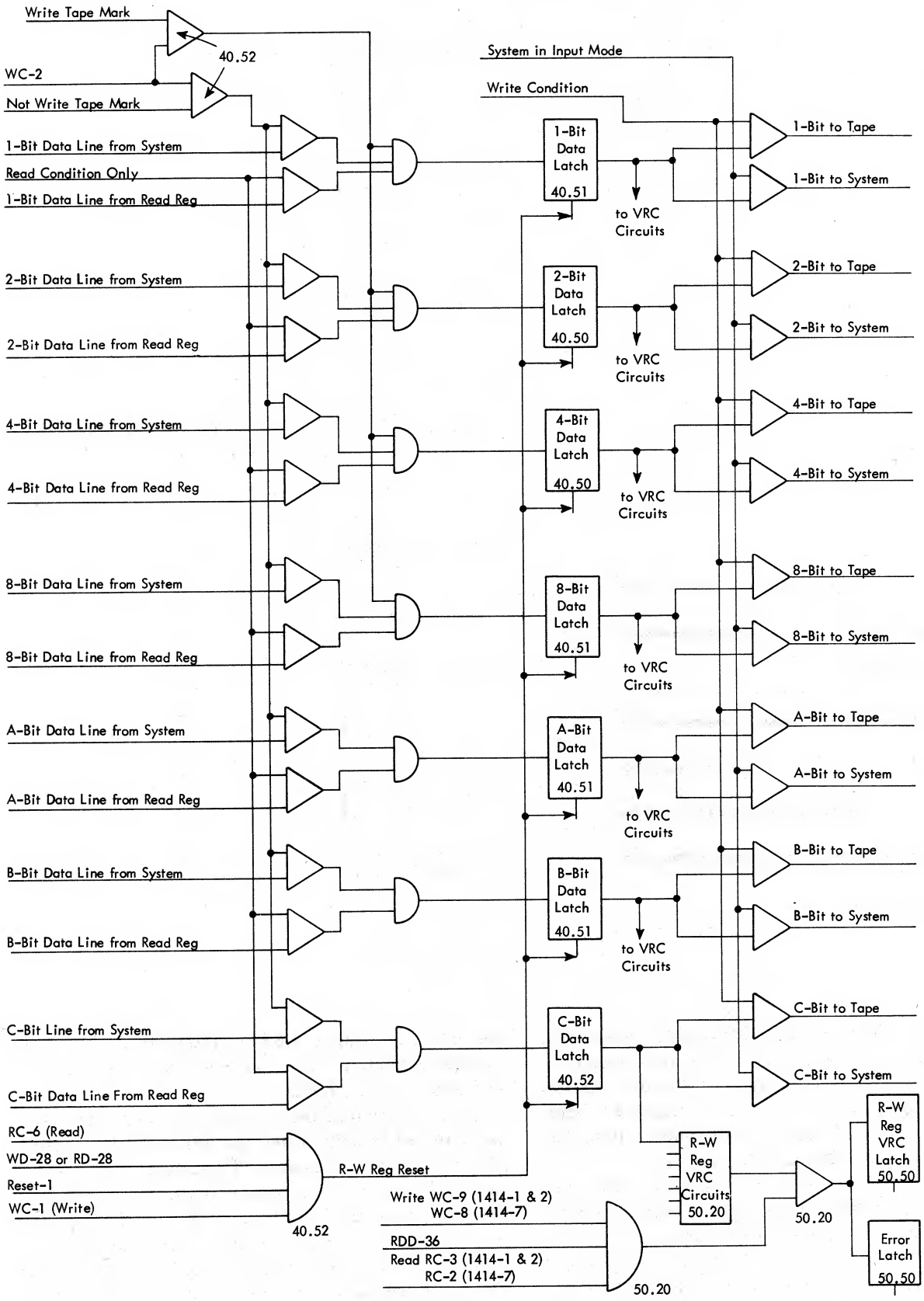


Figure 20. Read-Write Register

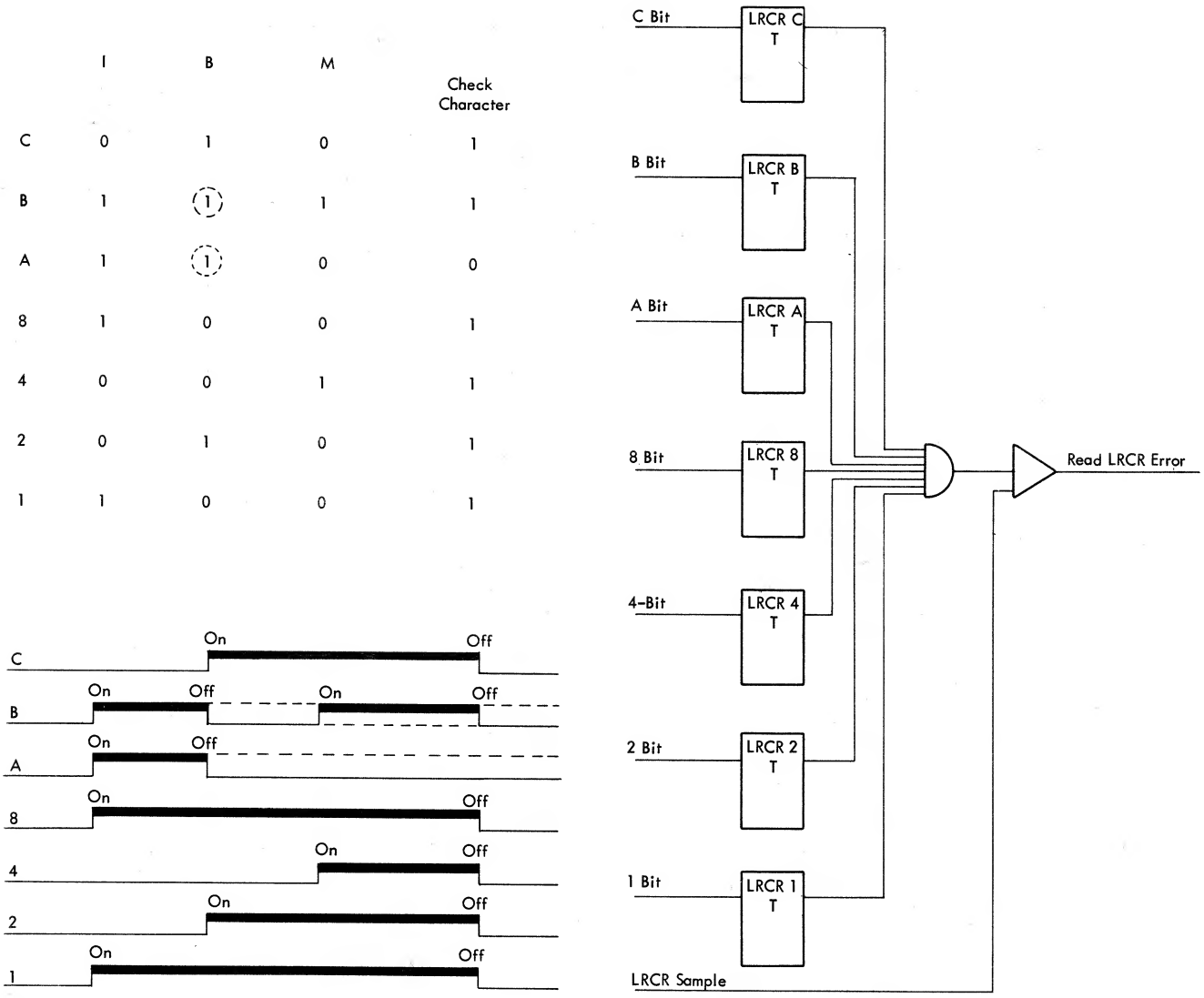


Figure 21. LRCR Check

parity. If the odd-even character counter shows that an odd number of characters have been recorded before the check character, the tape synchronizer checks the check character for odd or even parity as determined by the state of the odd redundancy latch. The following examples illustrate this action.

If the odd redundancy latch is on and a two character record is written on tape, the character counter shows that an even number of characters precede the check character in the record. If the bit structures of the characters are 1, 2, 4, 8, A, B, C and 1, 4, A, the bit structure of the check character is 2, 8, B, C. The odd redundancy latch is set; therefore, the first two characters of the record are checked for odd parity. Because the character counter shows an even count, the odd redundancy latch is reset when the check character latch is set, and the check character is checked for even parity.

If the odd redundancy latch is set and a three character record is written on tape, the character counter shows that an odd number of characters precede the check character in the record. If the bit structure of the characters are 1, 2, 4, 8, A, B, C ----1, 4, A, and 1, 4, 8, the bit structure of the check character is 1, 2, 4, B, C. The odd redundancy latch is set; therefore the first three characters of the record are checked for odd parity. Because the character counter shows an odd count, the check character is checked for the parity indicated by the odd redundancy latch. The check character is, therefore, checked for odd parity.

Vertical Redundancy Check (VRC)

Data from read register A and the read-write register condition VRC circuits to determine the vertical bit structure of a character. The correct vertical structure can be either odd or even, as designated by the status of the odd redundancy latch. To check a record in odd parity, the data channel or the processing unit must condition the "odd redundancy call" line to the tape synchronizer to turn on the odd redundancy latch. The output of the latch conditions the VRC circuits to indicate an error when the vertical bit structure of a character is even. When the latch is off, the VRC circuits indicate an error if the vertical bit structure of a character is odd. The following example illustrates this action.

If the character G (1-, 2-, 4-, A-, B-, and C-bits) is checked for even parity and one bit in the character has been dropped, a vertical redundancy error is indicated because the character then shows an odd bit count. If an even number of bits in the character are dropped, the vertical redundancy check circuits do not detect the error.

Echo Errors

At write clock-4 (WC-4) time in 1414-1 and 2 operation or at write clock-6 (WC-6) time in 1414-7 operation, the no echo latch is set. When the character processed during the current write clock cycle is written on tape, the tape unit develops an echo pulse; the echo pulse is sent to the tape synchronizer to reset the no echo latch. At WC-14 time in 1414-1 and 2 operation and at WC-2 time of the next write clock cycle in 1414-7 operation, the status of the no echo latch is examined. If the echo pulse from the tape unit has not reset the no echo latch, the no echo error and error latches are set. The echo pulse should reset the no echo latch before the write clock advances to WC-14 (1414-1 and 2) or to WC-2 of the next write clock cycle (1414-7). When the last character of the record is written in 1414-7 operation, the "WDD-60" pulse samples the status of the no echo latch.

Write Compare

The character in read register A is compared to the character in read register B in the read check of a tape write operation. Because the high-clip output of the final amplifiers set read register A and the low-clip output of the final amplifiers set read register B, the same character might not be stored in both registers. If the data in both read registers do not represent the same character and the Stop On Error CE switch is off, the compare check and error latches are set at RC-10 time. If the Stop On Error CE switch is on and an error is detected, the compare check and error latches are set at RC-6 time.

Write Delay Noise

In a 729 tape write operation, gates for the final amplifiers are conditioned during the write delay. However, no pulse should appear at the output of the final amplifiers before the write delay is terminated. Write delay noise circuits detect high-clip output pulses from the final amplifiers during the write delay. The ON output of the write delay latch combines with any high-clip pulse from the final amplifiers to set the write delay noise and error latches. For example, if the erase head on the tape unit has not destroyed a previously written record on tape, the 729 tape unit transfers data pulses to the tape synchronizer during the write delay. The write delay noise and error latches are set when such a condition occurs.

Because final amplifiers are not gated until the end of the write delay in 7330 tape write operations, the write delay noise circuits are ineffective in 7330 tape write operations.

Skew Error

Skew error circuits detect excessive speed variations in tape movement between the write and read heads on the tape unit. Should the tape driving mechanism skip or bind during a tape write operation, tape speed momentarily decreases. Because character spacing is a function of tape speed and writing frequency, variations in tape speed cause irregular character spacing. When tape speed decreases, less tape passes the write head, but the writing frequency is unchanged. Therefore, characters on tape are written closer together. When tape moves at normal speed again, intervals between the closely spaced characters are shorter than the time that the tape synchronizer requires.

In the read check of a tape write operation, the skew gate latch is set and reset during each read clock cycle. The skew error and error latches turn on when the ON output of the skew gate latch AND's with any high-clip bit from the final amplifiers after the allotted time for the character to arrive has elapsed.

Figure 22 illustrates the manner in which a skew error occurs and is detected. Graph A shows a typical tape envelope (ignoring starting time). Tape speed is constant to T5. Tape speed decreases after T5 and is normal after T9.

Graph B shows tape speed. Before T5 and after T9, the distance that tape travels is directly proportional

to time. Characters written at timed intervals are shown on the graph. Character spacing is shown at the right of the graph.

Chart C shows the action of the skew circuits when characters are read during the read check of a tape write operation. Only characters 4, 5, and 6 are represented. The first bit from the final amplifiers starts the read clock. Four clock steps are allotted for all bits of the characters to be read. Characters 5 and 6 are spaced closer than normal. Character 6 is read while the skew gate latch is set, causing the skew error and error latches to turn on.

Close character spacing is called "bit packing" or "character packing".

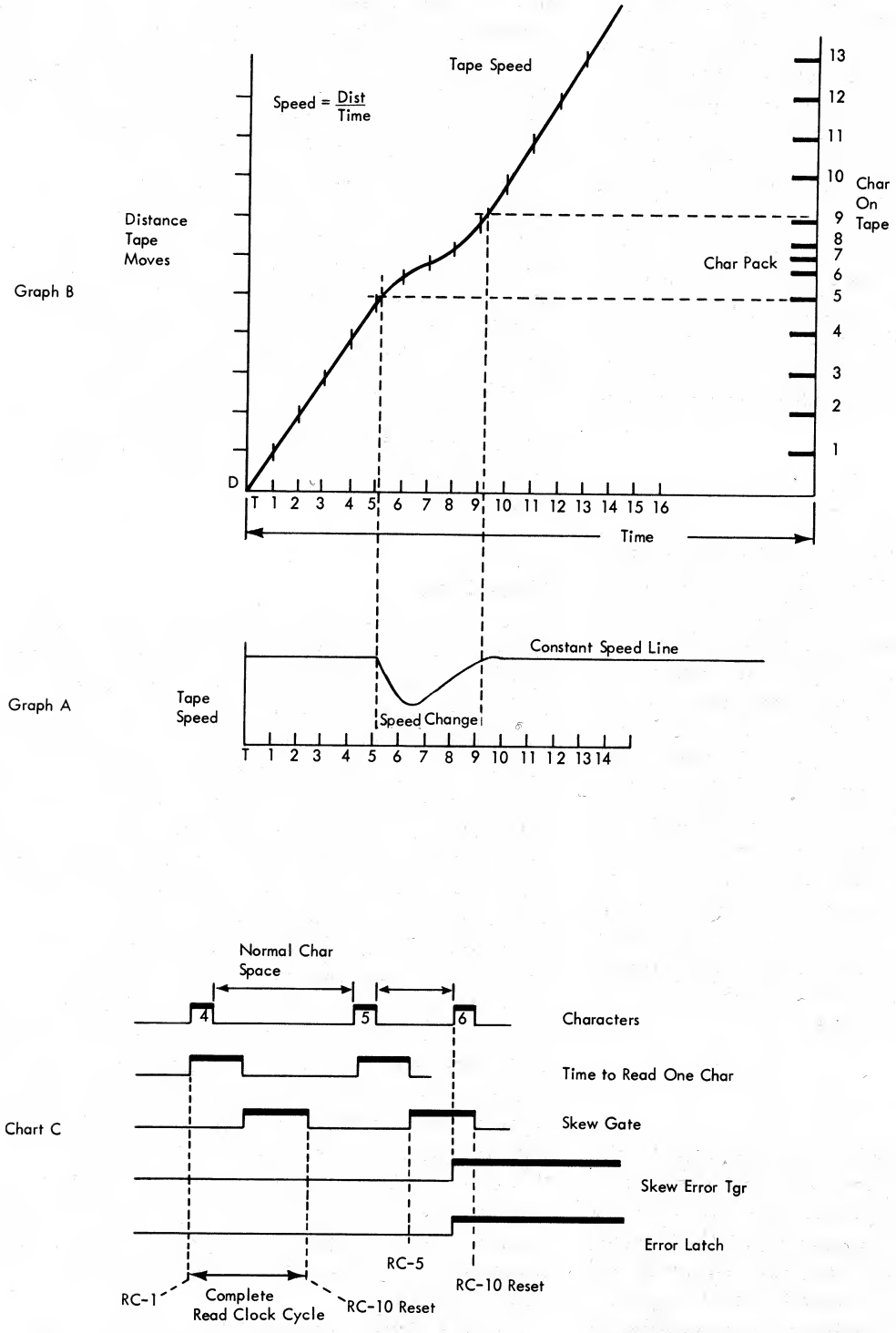


Figure 22. Skew Error and Check Circuits

Write

In a tape write operation, the system processes designated core storage characters (one at a time) through the tape synchronizer to the selected tape unit. The tape unit:

1. Records each character on magnetic tape.
2. Reads a character previously written on tape and transfers the character to the tape synchronizer to be checked.

The processing unit (1410/7010) or the data channel (7040/7044) transfers characters to the read-write register in the tape synchronizer. The tape synchronizer checks each character for a parity error and transmits the character to the tape unit to be recorded on magnetic tape. Because the tape synchronizer has the capacity to store only one character at a time, character transfers are controlled by the write clock in the tape synchronizer. During each write clock cycle, the tape synchronizer processes one character from the data channel (7040/7044) or processing unit (1410/7010) to the selected tape unit. The write clock cycles repetitively from the beginning of the write operation until the last character is transferred to the tape unit.

The write head on the tape unit writes characters received from the tape synchronizer on magnetic tape. As tape moves from the write head and passes the read head, characters are read and transferred to the tape synchronizer to be checked. The read clock in the tape synchronizer controls all tape synchronizer checking circuits. During each read clock cycle, the tape synchronizer checks one character written on tape earlier in the write operation. Each character from the tape unit starts the read clock; the clock completes one cycle and stops. The tape write operation is not complete until the last character in the tape record is checked. Figures 23, 24, 25, 26, and 27 show detailed tape synchronizer actions when executing the tape write operation.

Preliminary Conditions

In 1410 operation, execution of the M/L (%Un) (B)W instruction causes the processing unit to condition the write call line to the tape synchronizer. Execution of the M/L (%Un)(B)W instruction causes the processing unit in the 7010 System to condition "write call" to the tape synchronizer if the first character to be transferred from core storage is not a group mark word mark. In 7040/7044 operation, execution of the write select instruction causes the data channel to send the write call signal to the tape synchronizer. In all cases, "write call" initiates tape synchronizer actions in the write operation by setting latches (tape in process, write, and write delay) and by turning on all LRCR triggers.

When the tape in process latch is set, the 1410 or 7010 channel controlling the tape write operation cannot be used for any other I-O operation.

The write latch:

1. Conditions the tape busy line. When "tape busy" is active, the tape synchronizer cannot be designated to execute another tape operation. The data channel controlling the 7040/7044 tape write operation cannot communicate with other I-O devices until the complete record has been written and checked and "tape busy" drops.
2. Sets the tape unit to write status. The tape unit sends the "select, ready, and write" line to the tape synchronizer when the tape unit is in write status. If, however, the selected tape unit is in file protect status, the write latch output is blocked; write status is not set, and the write operation is not completed.

The write delay latch:

1. Conditions the write delay noise circuits. In 729 tape write operations, the tape synchronizer conditions the final amplifiers to process data at WD-32 time during the write delay. However, the tape unit should not transfer the first character in the tape record to the tape synchronizer before the write delay is terminated. Any high-clip output from the final amplifiers during the write delay sets the write delay noise and error latches. Because final amplifiers are not gated until the end of the write delay in 7330 tape write operations, write delay noise circuits are ineffective when a 7330 tape unit writes a record.
2. Sets the go latch. The output of the go latch causes the selected tape unit to move tape forward.
3. Conditions the delay counter for millisecond operation. The delay counter steps in the millisecond mode at a rate determined by the tape unit performing the write operation. Delay counter outputs combine with the output of the write delay latch, producing write delay (WD) timings. The write delay (WD) timings identify this period of the operation (the interval allowed for tape to reach proper operating

speed before writing begins) and establish times at which write delay actions occur.

When the delay counter advances to 28, the "WD-28" pulse tests the states of the LRCR triggers. If all LRCR triggers are on ("write call" set the LRCR triggers), the gate-on-final amplifiers latch is set, conditioning the gate for the first stage of the final amplifiers. Data are not processed through the final amplifiers, however, until the first and last stages are gated. Gating the final amplifiers by stages eliminates the possibility of noise transfer to the read registers in the read check of the write operation. If the gate-on-final amplifiers latch is set when the delay counter advances to 30, indicating that LRCR circuits are functioning properly, the WD-30 pulse resets the LRCR triggers and all error latches in the tape synchronizer.

If a 729 tape unit is selected to write the record:

and tape on the selected tape unit is not at load point, the read condition latch is set when the delay counter advances to 32.

and tape on the selected tape unit is at load point, the read condition latch is set when the delay counter advances to 96.

When the read condition latch is set, the gate for the last stage of the final amplifiers is conditioned, allowing the tape synchronizer to check each character written on tape.

If tape is at load point when the tape unit is selected, the load point latch is set, causing the WD-320 pulse (729) or the WD-1088 pulse (7330) to turn on the write condition latch. If tape is not at load point, the write condition latch is set when the delay counter advances to 50 (729) or to 72 (7330). Because tape is not positioned at the identical spot with respect to the write head after each load rewind operation, the longer delay when tape is at load point causes the tape unit to erase a section of tape (approximately 3¾ inches) before writing the first record. This ensures that all previously recorded data on tape are destroyed before the new record begins.

Between the times that the go latch starts tape movement and the write condition latch permits writing to begin, tape reaches proper operating speed.

The write condition latch:

1. Sets the write trigger release latch, allowing write triggers in the selected tape unit to turn on and off as required to record characters on tape. When the write trigger release latch is reset (after the last normal character in the record is processed), write triggers write the check character at the end of the tape record.

2. Sets the read condition latch when a 7330 tape unit performs the write operation. When the read condition latch is set, the gate for the last stage of the final amplifiers is conditioned, allowing the tape synchronizer to check each character written on tape.

3. Starts the write clock. The write clock establishes timings that control data flow through the tape synchronizer to the tape unit. When the write condition latch is set, the write clock cycles continuously.

Data Transfers

The read-write register is reset at write clock-1 (WC-1) time. The write delay latch and the delay counter are reset at write clock-1 (WC-1) time in 1414-1 and 2 operation or at write clock-2 (WC-2) time in 1414-7 operation.

At WC-2 time, input data lines to the tape synchronizer from the processing unit (1410/7010) or data channel (7040/7044) are sampled. Active data lines set corresponding read-write register data latches. The read-write register conditions output data lines to the tape unit.

The tape synchronizer conditions "tape write strobe" to the processing unit (1410/7010) or data channel (7040/7044) at WC-4 time, indicating that the tape synchronizer has received a character from the system; the character is in the read-write register and has not been processed at this time, however. The system can now transmit the next character to the tape synchronizer, but the tape synchronizer will not accept the character until WC-2 time of the next write clock cycle.

In 1414-1 and 2 operation, the WC-4 pulse sets the no echo latch. In 1414-7 operation, the WC-6 pulse sets the no echo latch.

From WC-4 to WC-8 time, the tape synchronizer conditions the write pulse line to the selected 7330 tape unit. The trailing edge of "write pulse" (at WC-9 time) causes the 7330 tape unit to write the character designated on the read-write register output lines.

At WC-9 time (1414-1 and 2) or WC-8 time (1414-7):

1. The tape synchronizer transmits "write pulse" to the selected 729 tape unit. The leading edge of "write pulse" causes the 729 to write the character designated on the output lines from the read-write register.

2. The tape synchronizer checks the character in the read-write register for a vertical redundancy error. The status of the odd redundancy latch determines whether a character is checked for odd or even redundancy. The "odd redundancy call" from the system sets the odd redundancy latch, specifying that all characters in the record should be checked for odd parity. If the system has not conditioned "odd redundancy call," the tape synchronizer checks characters for even parity (even number of bits in the character).

When all other characters, except the check character, are written on tape, the tape unit develops an

echo pulse; the tape unit transmits the echo pulse to the tape synchronizer to reset the no echo latch (set at WC-4 or WC-6 time). In 1414-1 and 2 operation, the echo pulse must reset the no echo latch before the write clock advances to 14. In 1414-7 operation, the echo pulse must reset the latch before WC-2 time of the next write clock cycle or before write disconnect delay-60 (WDD-60) time of the disconnect operation. If the no echo latch is not reset in the required time, the no echo error latch and the error latch are set.

"Disconnect call" from the system turns on the disconnect latch in the tape synchronizer. The tape synchronizer tests the state of the disconnect latch at WC-14 time of each write clock cycle. If the latch is off, the write clock advances to 15 to complete the cycle and begins another clock cycle to transfer the next character in the tape record to the tape unit. If the disconnect latch is set at WC-14 time, the tape synchronizer initiates the write circuits disconnect operation.

Write Circuits Disconnect

The ON output of the disconnect latch combines with the WC-14 pulse to reset the write condition latch and set the write disconnect delay latch. When the write condition latch resets, the write clock-8 trigger conditions the write clock oscillator drive pulses to complete the clock cycle and stop with all clock triggers off.

Outputs of the write trigger release and write disconnect delay latches condition the delay counter for microsecond operation. The selected tape unit and the density at which the tape unit is writing select oscillator drive pulses. Delay counter outputs combine with the output of the write disconnect delay latch to provide write disconnect delay (WDD) timings.

When the delay counter advances to 60, the WDD-60 pulse:

1. Resets the write trigger release latch. The level shift at the output of the latch resets the write triggers in the tape unit, causing the tape unit to write the check character. If all write triggers in the tape unit are off when the write trigger release latch is reset, the tape unit does not write a check character. (Theoretically, the check character has no bits.) Because of the extended delay before the tape unit writes the check character (WDD-60 time), the check character is spaced further from the last normal character in the record than normal character spacing.
2. Resets the delay counter.

The OFF output of the write trigger release latch and the ON output of the write disconnect delay latch combine to condition the delay counter for millisecond operation. When the delay counter advances to 20, the "WDD-20" pulse resets the write disconnect delay latch, the delay counter, and, if a 729 tape unit is performing the tape write operation, the go latch. Because the read check of the write operation is not complete when the tape unit writes the check character, the WDD-20 delay allows tape movement on a 729 unit to proceed at full speed until the check character passes the read head.

Read Check of Write Operation

As the tape moves from the write head to the read head on the tape unit, each character written in the write operation is read and transferred to the tape synchronizer to be checked. Read check circuits in the tape synchronizer can process a character from the tape unit after the read condition latch is set, but the read check operation cannot begin until the first character in the record moves to the read head on the tape unit.

FIRST BIT

Because tape units move tape at different speeds and can operate at more than one density, no predetermined time is set for each character to be read. The tape unit transmits characters to the final amplifiers in the tape synchronizer. Final amplifiers have high-clip and low-clip outputs. The tape synchronizer initiates check operations on the character when the character's first high- or low-clip bit is detected at the output of the final amplifiers. The first bit (high- or low-clip) from the final amplifiers sets the first bit latch. The first bit latch unclamps read clock oscillators and allows the read clock to run for one clock cycle. Check operations on the character must end and the read clock must be reset before the first bit of the next character from the tape is detected at the output of the final amplifiers.

DATA FLOW AND ERROR CHECKS

High-clip outputs from final amplifiers set read register A; low-clip outputs from final amplifiers set read register B. The skew gate latch is set:

at RC-4 time if the tape unit writing the record is recording at any other density except 800 cpi.
at RC-5 time if a 729 V tape unit is performing the write operation in the 800 cpi density mode.
at RC-6 time if a 729 VI tape unit is performing the write operation in the 800 cpi density mode.

The complete character should be stored in the read registers when the read clock sets the skew gate latch. While the skew gate latch is set, any high-clip pulse from the final amplifiers turns on the skew error and

error latches. The skew check detects characters spaced too closely on tape.

The tape synchronizer checks the character stored in read register A for a vertical redundancy error. If no error is detected, the RC-5 pulse (1414-1 and 2) or RC-7 pulse (1414-7) loads the LRCR with the character in read register A. If a vertical redundancy error is detected in the character in read register A:

1. The RC-5 pulse (1414-1 and 2) or RC-6 pulse (1414-7) sets the A register VRC latch. The A register VRC latch sets the error latch.
2. The RC-5 pulse (1414-1 and 2) or RC-7 pulse (1414-7) loads the LRCR with the character in read register B.

Although the LRCR is loaded with the character in read register A or read register B at RC-5 or RC-7 time, the character remains in both read registers. The character in read register A is compared to the character in read register B. If both registers do not contain the same character, the compare check and error latches are set at RC-10 time.

The read clock generates a reset pulse at the end of RC-10 time. The RC-10 reset pulse resets the skew gate latch, read register A, read register B, the first bit latch, and the read clock. When the first bit latch is reset, read clock oscillators are clamped preventing the read clock from taking another cycle until the next character is received from the tape unit.

Timings in the write and read check circuits are set so that the write condition and write disconnect delay latches are reset when the last normal character in the record is checked; this allows the output from the read clock at RC-5 time (1414-1 and 2) or RC-7 time (1414-7) to set the read disconnect delay latch. The read disconnect delay latch conditions the delay counter for microsecond operation. Outputs of the delay counter combine with the output of the read disconnect delay latch, providing read disconnect delay (RDD) timings after the last normal character in the record is checked.

CHECK CHARACTER

The check character is the last character of the record and is spaced further from the preceding character than normal character spacing. Because of the extended delay before the check character is read, the delay counter advances to 36 and turns on the check character latch before check character bits can be sent to the tape synchronizer. The delay counter runs throughout the check character cycle.

The check character may or may not have bits depending on the status of the write triggers in the tape unit when the write trigger release latch was reset. If the check character does not have bits, the read clock does not run during the check character cycle; delay counter outputs complete the read check of the record, reset all tape synchronizer circuits, and terminate the tape write operation.

Check character bits are processed through the final amplifiers and the read register as normal character bits. The skew gate and read register A vertical redundancy check circuits function as in normal character operation. If a vertical redundancy error is detected in the check character in read register A, the LRCR is loaded with the check character in read register B, but the A register VRC and error latches are not set. The check character in read register A is compared to the check character in read register B. If both registers do not contain the same character, the compare check and error latches are set at RC-10 time. The reset pulse at the end of RC-10 time resets the skew gate latch, read register A, read register B, the first bit latch, and the read clock.

Tape Write Operation Disconnect

The tape write operation can be terminated when the read check circuits process the check character. Read disconnect delay pulses provide timings to check the LRCR and reset all circuits in the tape synchronizer. Because 729 and 7330 tape units have different characteristics, disconnect procedures for the two types of tape units differ; however, both procedures accomplish the same result.

729 DISCONNECT

The RDD-128 pulse resets the read condition latch, causing the gate for the last stage of the final amplifiers to become inactive. At RDD-136 time, the LRCR is sampled for errors. All LRCR triggers should be off; if one or more LRCR triggers are on, indicating that bits have been picked up or dropped, the error latch is set.

The RDD-144 pulse resets the tape in process latch and conditions the RDD-144 reset line.

The 1410 or 7010 channel committed to the write operation is disconnected when the tape in process latch is reset.

The RDD-144 reset line turns off:

1. The load point latch.
2. The check character latch.
3. The disconnect latch.
4. The delay counter.
5. The gate-on-final amplifiers latch.
6. The odd redundancy latch.
7. The write latch.
8. The erase latch.
9. The write tape mark latch.
10. The read disconnect delay latch.

When the write latch is reset, "tape busy" drops free-

ing the tape synchronizer to control another tape operation. In 7040/7044 operation, the data channel that initiated the tape write operation is disconnected when "tape busy" drops.

7330 DISCONNECT

At RDD-110 time:

1. The read condition latch is reset.
2. The read disconnect delay latch is reset.
3. The delay counter is reset.
4. The LRCR is sampled for errors. All LRCR triggers should be off; if one or more LRCR triggers are on, indicating that bits have been picked up or dropped, the error latch is set.
5. The forward-stop delay latch is set.

The forward-stop delay latch conditions the delay counter for millisecond operation. Delay counter outputs combine with the output of the forward-stop delay latch, providing forward-stop delay (FSD) timings.

The FSD-1 pulse (1414-1 and 2) or FSD-2 pulse (1414-7) conditions the compute line. Compute resets the tape in process latch, allowing the 1410 or 7010 channel to disconnect from the tape write operation. No other tape operation requiring use of the tape synchronizer can be initiated, however, until "tape busy" drops.

The FSD-44 pulse conditions the RDD-144 reset line although the delay counter has only advanced to 44. "RDD-144 reset" turns off:

1. The load-point latch.
2. The check character latch.
3. The disconnect latch.
4. The delay counter.
5. The gate-on-final amplifiers latch.
6. The odd redundancy latch.
7. The write latch.
8. The erase latch.
9. The write tape mark latch.
10. The forward-stop delay latch.
11. The go latch.

When the write latch is reset, the tape busy line drops freeing the tape synchronizer to control another tape operation. In 7040/7044 operation, the data channel that initiated the tape write operation is disconnected when "tape busy" drops.

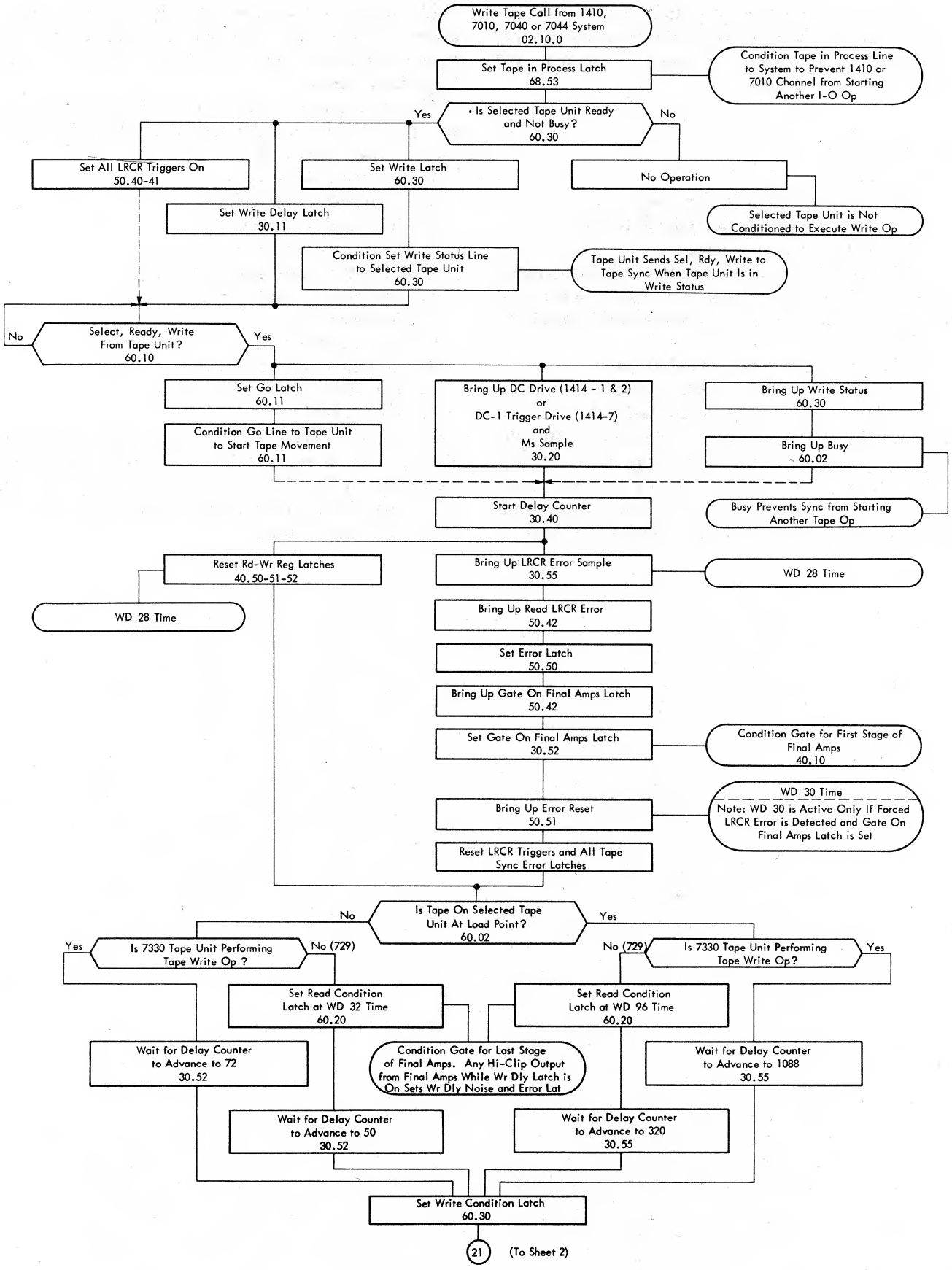


Figure 23. Tape Write Operation (Sheet 1 of 4)

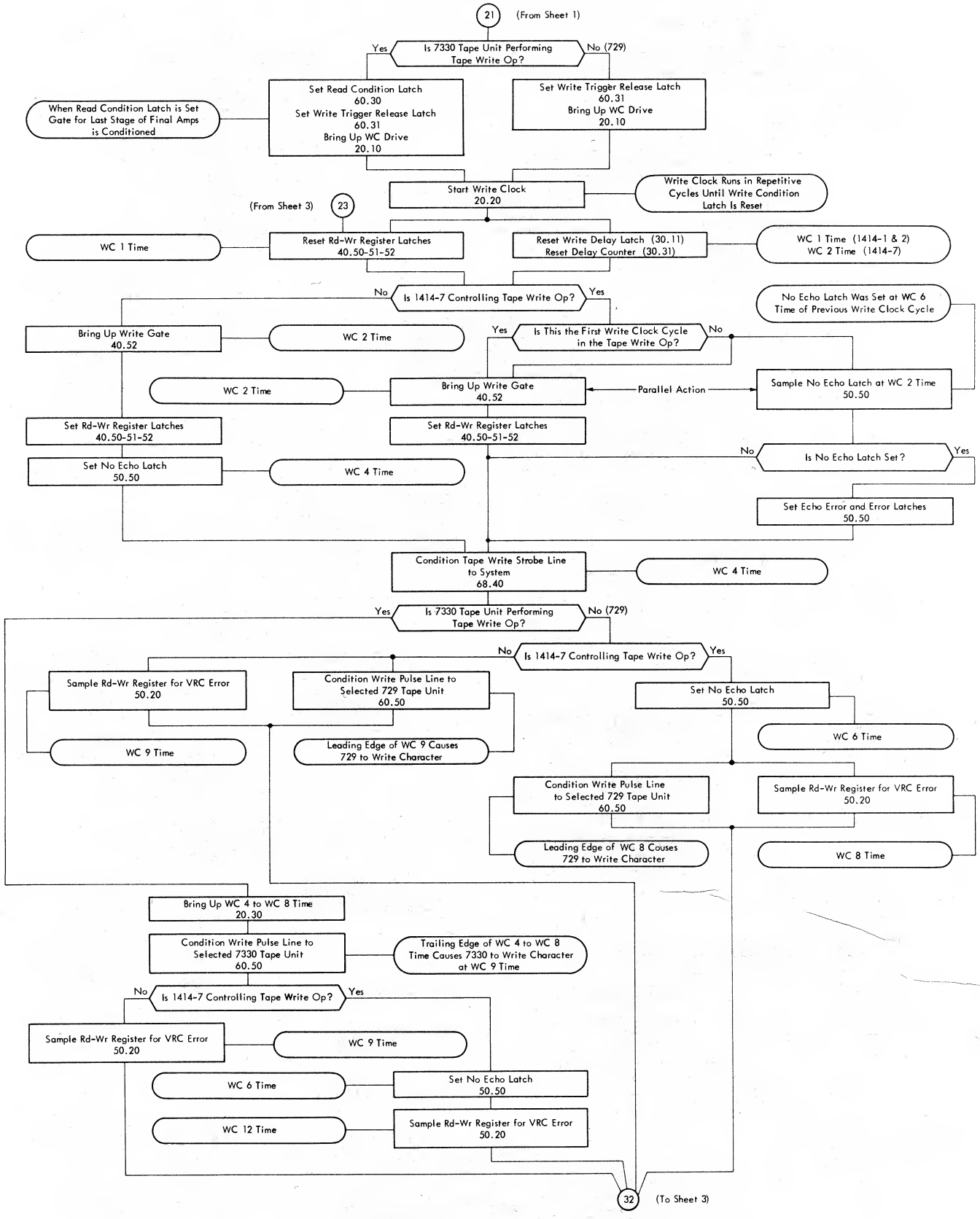


Figure 23. Tape Write Operation (Sheet 2 of 4)

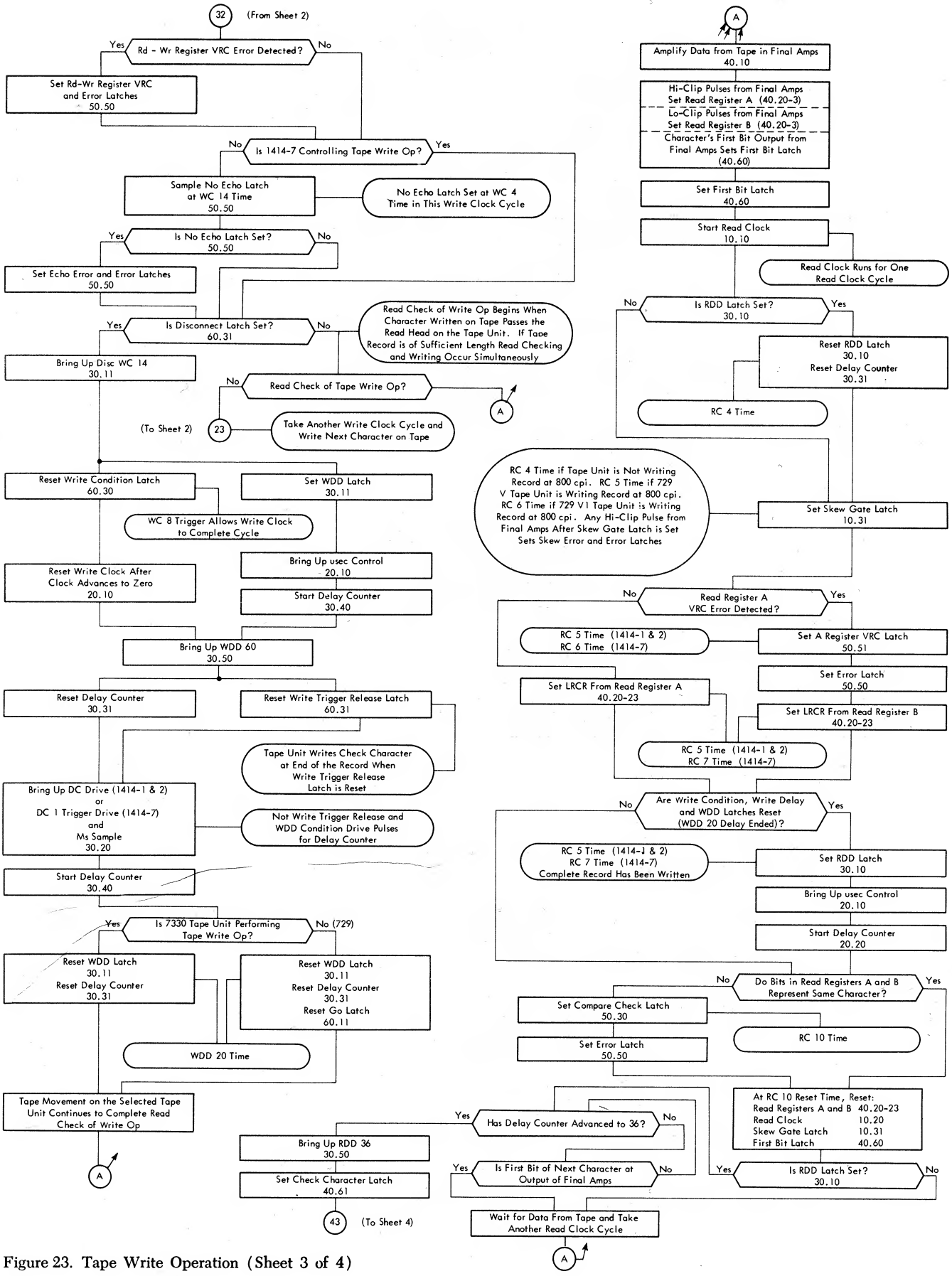


Figure 23. Tape Write Operation (Sheet 3 of 4)

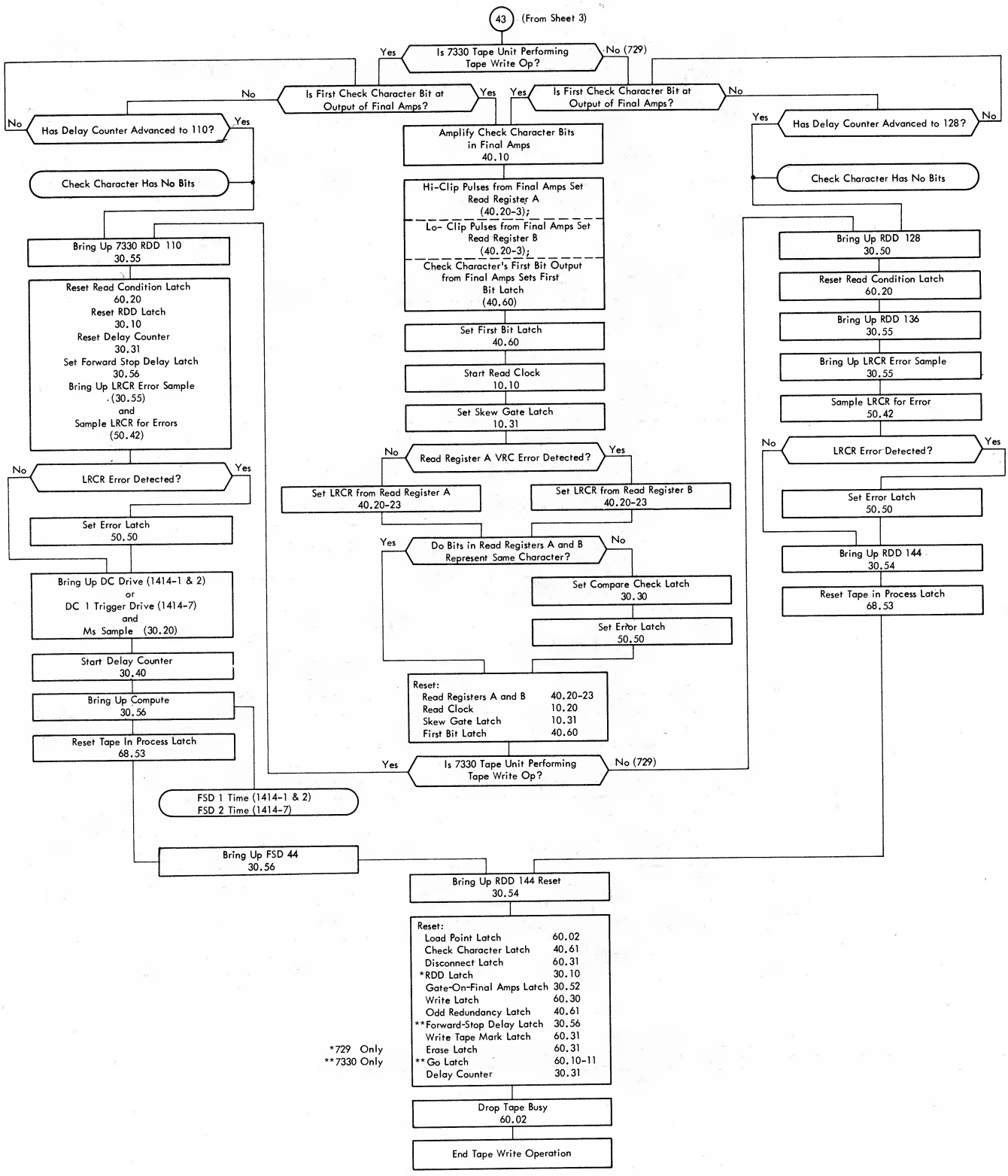
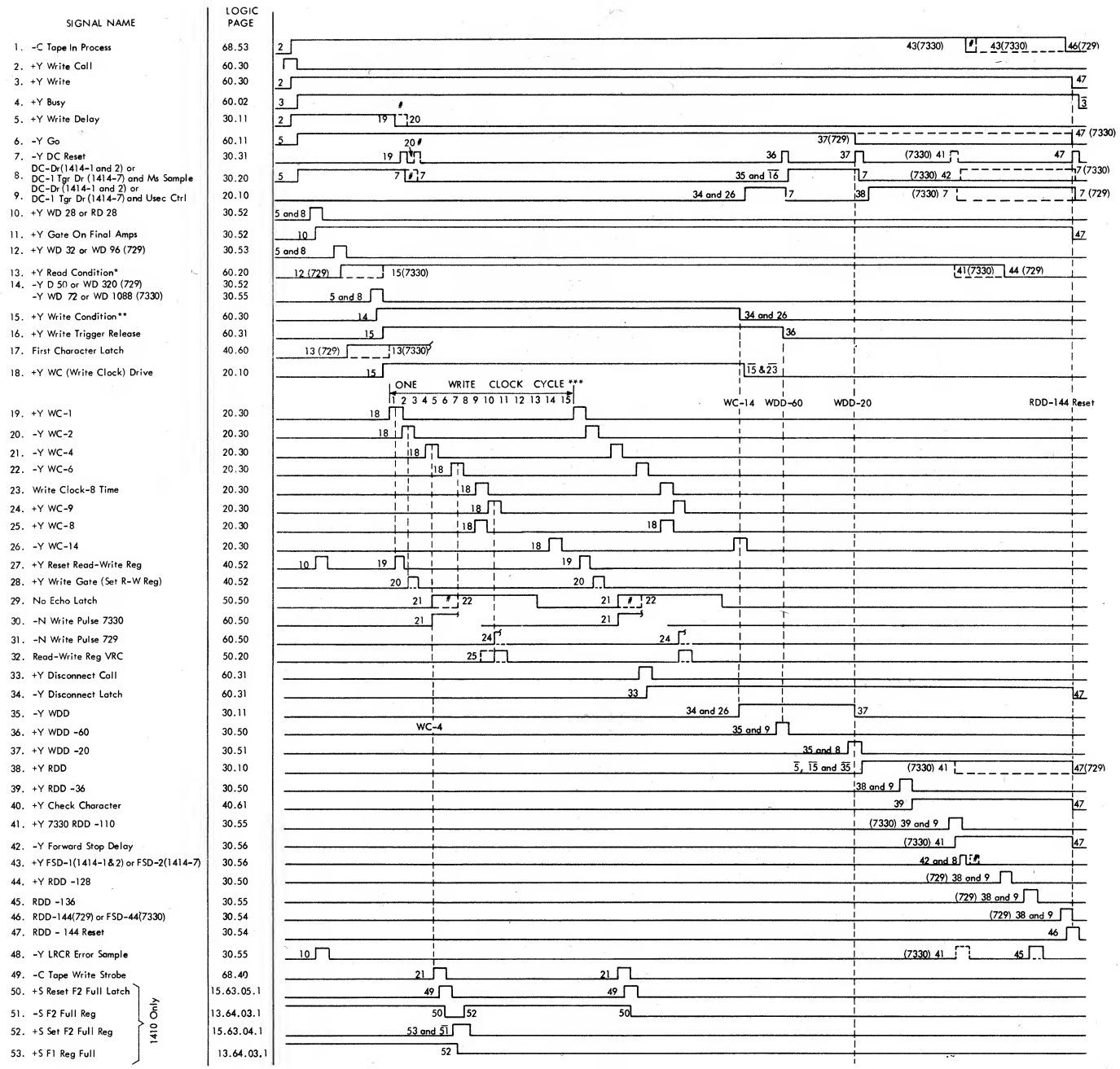


Figure 23. Tape Write Operation (Sheet 4 of 4)



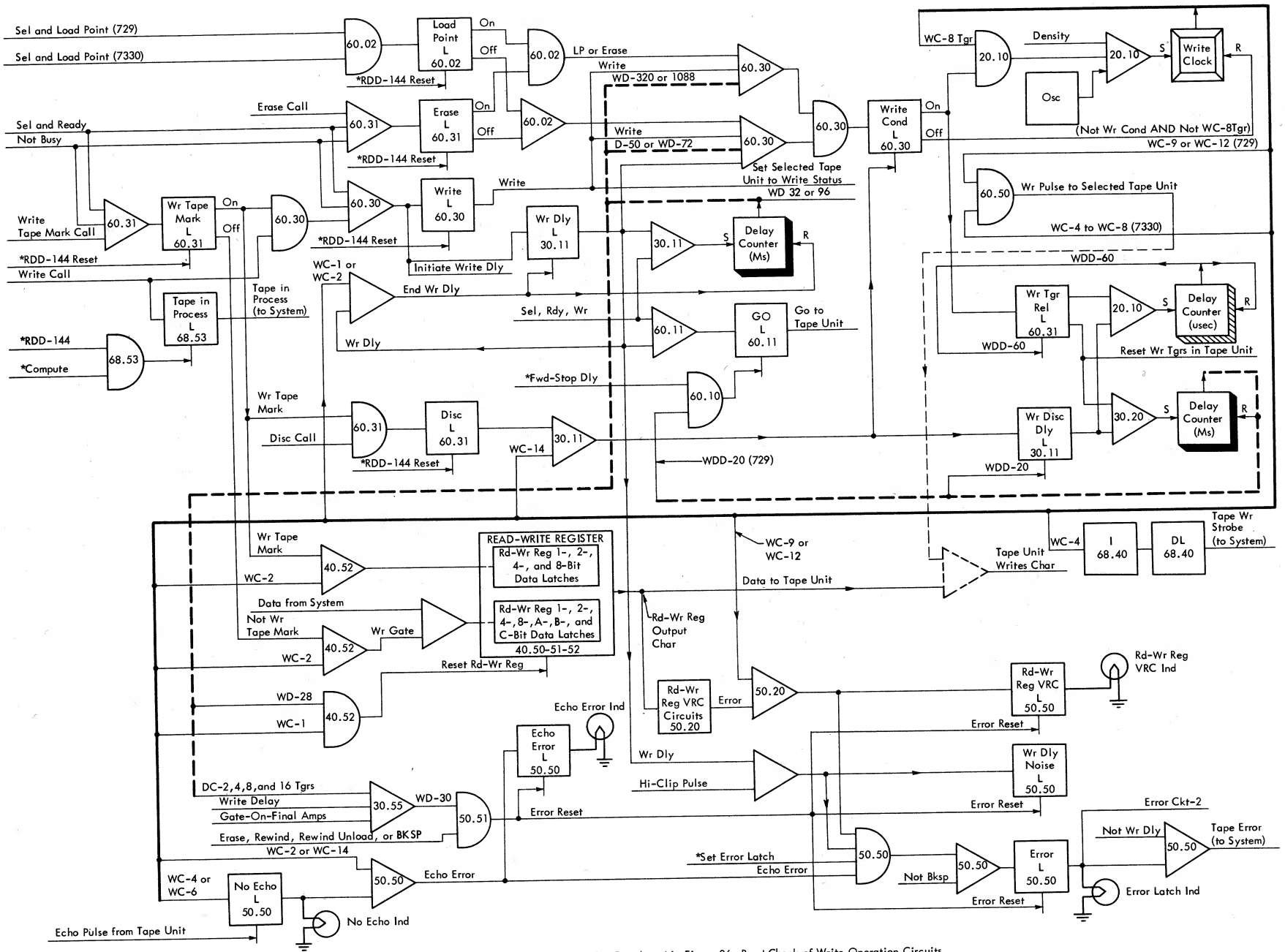
\# 1414-7 operation

* If load point latch is off, the WD-32 pulse sets the read condition latch in 729 operation;
if load point latch is set, the WD-96 pulse sets the read condition latch in 729 operation.

** If load point latch is off, the WD-72 pulse sets the write condition latch in 7330 operation; the D-50 pulse sets the write condition latch in 729 operation.
If load point latch is set, the WD-1088 pulse sets the write condition latch in 7330 operation; the WD-320 pulse sets the write condition latch in 729 operation.

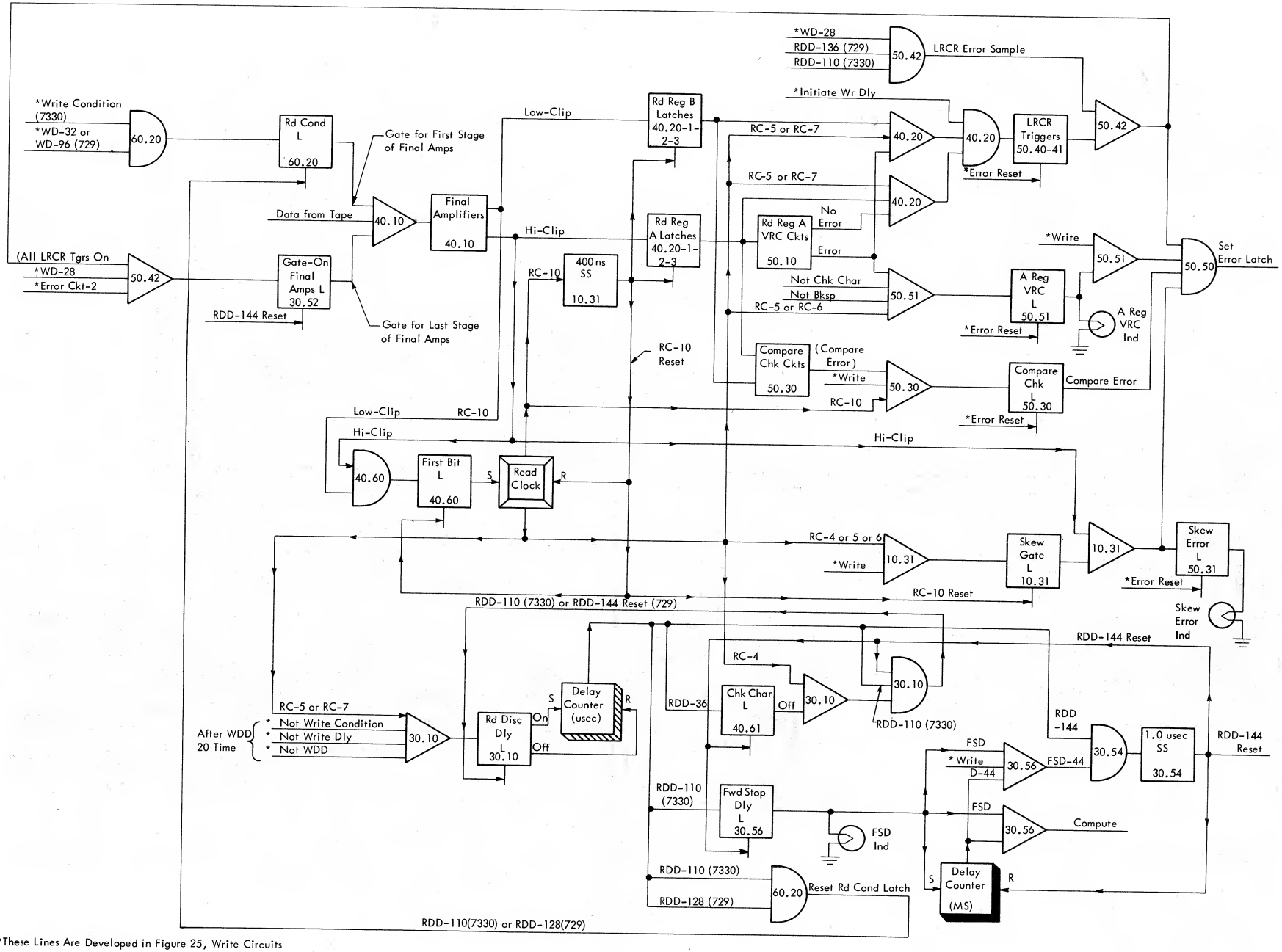
*** Write clock triggers reset (WC-0) before next WC-1 pulse is active; this is not shown.

Figure 24. Tape Write Timings



*These Lines Are Developed in Figure 26, Read Check of Write Operation Circuits

Figure 25. Write Circuits



*These Lines Are Developed in Figure 25, Write Circuits

Figure 26. Read Check of Write Operation Circuits

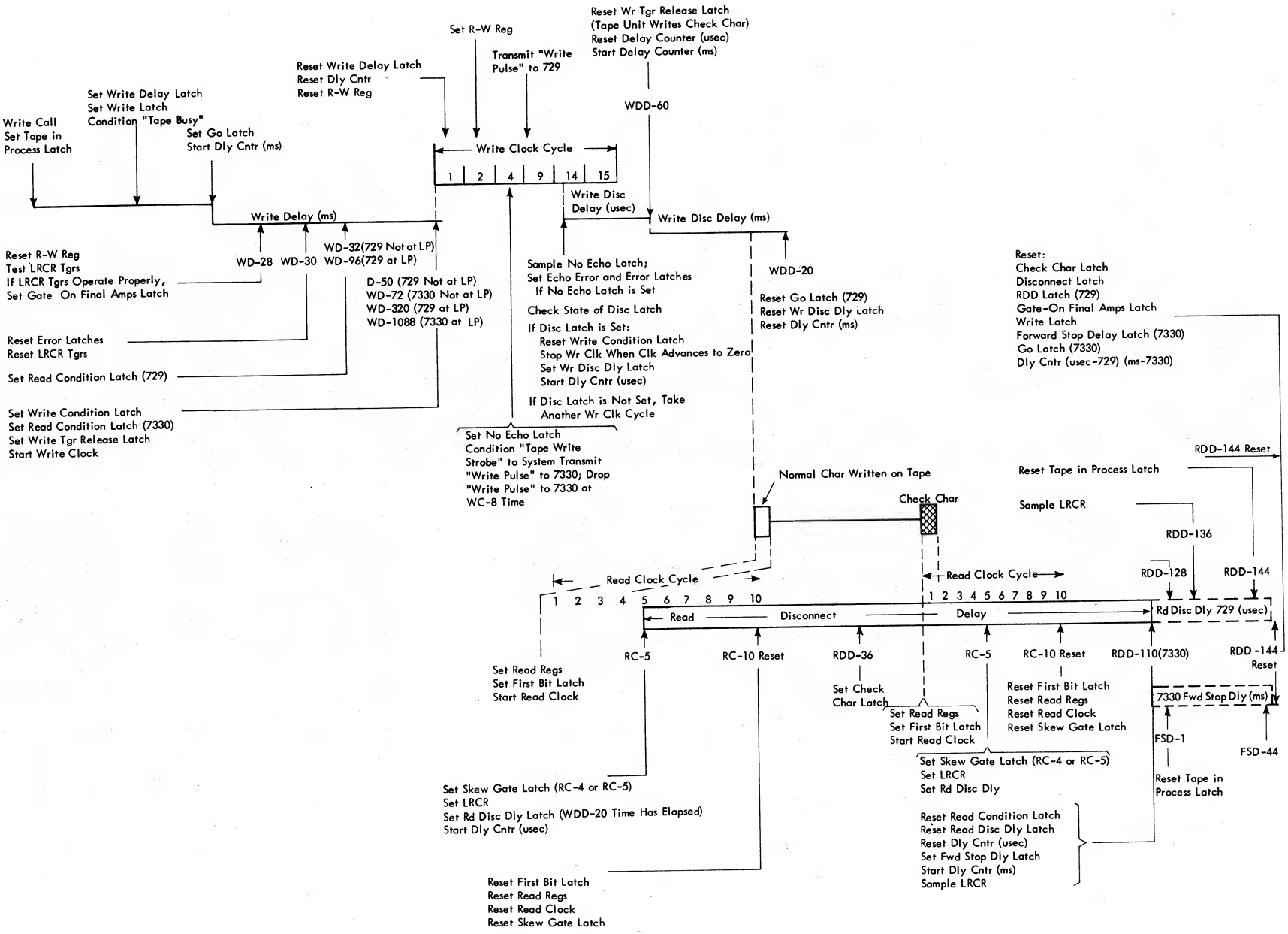


Figure 27. Simplified Write Operation Sequence

Read

In a tape read operation, the selected tape unit reads characters from tape and transfers the data (one character at a time) to the tape synchronizer. The tape synchronizer checks each character and processes the data to the processing unit (1410/7010) or data channel (7040/7044). The tape read operation is quite similar to the read check action in a tape write operation; in a tape read operation, however, characters are transferred to the system.

The read clock controls all checking circuits in the tape synchronizer. During all other read clock cycles except the cycle on which the check character is processed, the tape synchronizer processes one character to the system. Each character from tape starts the read clock; the clock runs for one clock cycle. The delay counter is conditioned at the end of the read clock cycle. If the tape unit transfers the next character to the tape synchronizer soon enough a read clock output in the subsequent read clock cycle resets the delay counter. The check character is spaced further from the preceding character in the record than normal character spacing. When the tape unit reads the last character in the record, the delay counter advances far enough to initiate the tape read disconnect operation before the check character arrives at the tape synchronizer. The tape synchronizer does not transfer characters to the system after the disconnect operation begins. Figures 28, 29, 30, and 31 show detailed tape synchronizer actions when executing the tape read operation.

Preliminary Conditions

The read select instruction to the 7040/7044 systems or the M/L (%Un)(B)R instruction to the 1410/7010 system causes the designated channel to condition "read call" to the tape synchronizer to begin a tape read operation. "Read call" turns on the tape in process, read only, and read delay latches and sets all LRCR triggers.

When the tape in process latch is set, the 1410/7010 channel controlling the tape read operation cannot be used in any other I-O operation.

The read only latch:

1. Conditions the tape busy line. When "tape busy" is active, the tape synchronizer cannot be designated to execute another tape operation. The data channel controlling the 7040/7044 tape read operation cannot communicate with other I-O devices until "tape busy" drops at the end of the read operation.

2. Sets the tape unit to read status. The tape unit sends the select, ready, and read line to the tape synchronizer when the tape unit is in read status.

The read delay latch:

1. Sets the go latch. The output of the go latch causes the selected tape unit to move tape forward.

2. Conditions the delay counter for millisecond operation. The delay counter steps in the millisecond mode at a rate determined by the tape unit performing the read operation. Delay counter outputs combine with the output of the read delay latch producing read delay (RD) timings. The RD timings identify this period of the read operation (the interval allowed for tape to reach proper operating speed) and establish times at which read delay actions occur.

When the delay counter advances to 28, the RD-28 pulse tests the states of the LRCR triggers. If all LRCR triggers are on ("read call" set the LRCR triggers), the gate-on-final amplifiers latch is set, conditioning the gate for the first stage of the final amplifiers. Data are not processed through the final amplifiers, however, until the first and last stages are gated. Gating the final amplifiers by stages eliminates the possibility of noise transfer to the read registers. If the gate-on-final amplifiers latch is set when the delay counter advances to 30, indicating that LRCR circuits are functioning properly, the WD-30 pulse resets the LRCR triggers and all error latches in the tape synchronizer.

If tape is at load point when the tape unit is selected, the load point latch is set, causing the RD-160 pulse (729) or the RD-768 pulse (7330) to turn on the read condition and first character latches. If tape is not at load point, the RD-44 pulse (729) or RD-36 pulse (7330) sets the read condition and first character latches. Regardless of the position of tape when the tape unit is selected, the delay in the read operation is shorter than the corresponding delay in the write operation to insure that read circuits are conditioned soon enough to read the first character of the record.

The first character latch conditions the tape mark recognition circuits to examine the bit configuration of the first character of the record. When the TI light is on, the tape unit returns the select and TI on line to the tape synchronizer to reset the turn on TI latch.

The read condition latch:

1. Conditions the gates for the read-write register and the last stage of the final amplifiers. The tape synchronizer can then accept characters from the tape unit.

2. Resets the read delay latch and the delay counter.

Between the times that the go latch starts tape movement and the read condition latch conditions the tape synchronizer to accept characters from tape, tape reaches proper operating speed.

Data Flow and Error Checks

Because tape units move tape at different speeds and can operate at more than one density, no predetermined time is set for the tape unit to read and transfer characters to the tape synchronizer. The selected tape unit transmits characters to the final amplifiers in the tape synchronizer. The final amplifiers have high-clip and low-clip outputs. The tape synchronizer initiates check operations on the character received from the tape unit when the character's first high-clip bit is detected at the output of the final amplifiers. The first high-clip bit from the final amplifiers sets the first bit latch. The first bit latch unclamps the read clock oscillators and allows the read clock to run for one clock cycle. The tape synchronizer sends the character to the system and resets the read clock before the first bit of the next character from tape is detected at the output of the final amplifiers.

High-clip outputs from the final amplifiers set read register A; low-clip outputs from the final amplifiers set read register B. The tape synchronizer checks the character in read register A for a vertical redundancy error. If no error is detected, the RC-7 pulse loads the read-write register and the LRCR with the character in read register A. If a vertical redundancy error is found in the character in read register A, the RC-6 pulse (1414-7) or RC-7 pulse (1414-1 and 2) set the A register VRC latch, and the "RC-7" pulse unconditionally loads the read-write register and the LRCR with the character in read register B. When the read-write register data latches are set, the tape synchronizer conditions corresponding data lines to the system. When the tape synchronizer is used with 7040/7044 systems, the high and low clip outputs are compared. The presence of only a low clip pulse (indicating a weak bit) sets the first bit latch. This insures that a weak one-bit character will not be skipped over.

At RC-7 time, the read disconnect delay latch is set, causing:

1. The 1414-7 tape synchronizer to condition the tape read strobe line to the system. In 1414-1 and 2 operation, the tape synchronizer does not condition "tape read strobe" until RC-3 time of the following read clock cycle. "Tape read strobe" is not active on the first read clock cycle of the tape read operation because the read disconnect delay latch is not set at the first RC-3 time. "Tape read strobe" signals the system that the tape synchronizer has processed a character and conditioned output data lines to the system. If the system does not accept the character before RC-6 time (the time at which the read-write register is reset), the character is lost.
2. The delay counter to advance in the microsecond mode.

Outputs of the delay counter combine with the output of the read disconnect delay latch, providing read disconnect delay (RDD) timings. The RC-4 pulse of the subsequent read clock cycle resets the read disconnect delay latch and the delay counter if the delay counter has not advanced to 36. If, however, the delay counter advances to 36 before the RC-4 pulse resets the read disconnect delay latch, the disconnect operation begins. The first bit of the following tape character should arrive at the tape synchronizer soon enough to advance the read clock to RC-4 before the delay counter steps to 36. The delay counter should advance to 36 only during the delay that the tape unit requires to read and transmit the check character to the tape synchronizer. When this delay occurs, the RDD-36 pulse conditions "tape read strobe" to the system in 1414-1 and 2 operation, allowing the last normal character in the record to be transferred from the tape synchronizer to the system.

The read clock generates a reset signal at the end of RC-7 time. The RC-7 reset pulse resets the first bit latch, read register A, and read register B. The OFF output of the first bit latch clamps the read clock oscillators, preventing the read clock from taking another cycle until the next character from the tape unit is received in the final amplifiers. During read clock reset time, when the 7040/7044 system is used, a read skew check is made. If a high clip pulse is detected during the read clock reset, the master error latch is set. Thus because of the more stringent requirements of the 7040/44 during a tape read operation, any excessive deviation of recorded bits is detected.

At RC-3 time (1414-1 and 2) or RC-2 time (1414-7) of the following read clock cycle, the tape synchronizer checks the character set in the read-write register during the previous read clock cycle for a vertical redundancy error. If an error is detected, the read-write register VRC and error latches are set. Because the first character of the record is not in the read-write register at RC-2 or RC-3 time of the first clock cycle, no read-write register vertical redundancy check is made at that time. The first character is checked for a read-write register vertical redundancy error during the second clock cycle; the second character is checked during the third clock cycle; the last normal character of the record is checked during the check character cycle. The read-write register is reset at RC-6 time, destroying the character stored in the register during the previous clock cycle.

Check Character

The check character is the last character of the record and is spaced further from the preceding character than normal character spacing. Because of the extended delay before the tape unit reads the check

character, the delay counter advances to 36 before the tape unit transfers the check character to the tape synchronizer. The RDD-36 pulse sets the check character latch, blocking the normal reset path to the read disconnect delay latch at RC-4 time.

Check character bits are processed through the final amplifiers and the read registers as normal character bits, but the check character is not loaded in the read-write register. Read register A is checked for a vertical redundancy error. If no error is detected, the check character in read register A is loaded in the LRCR. If an error is detected, the LRCR is loaded with the check character in read register B, but the A register VRC latch is not set. Because the check character is not transmitted to the system, the output of the check character latch blocks the input to the read-write register.

The read clock does not run during the check character cycle if the check character does not have bits. The last normal character of the record (set in the read-write register during the previous clock cycle) is checked for a read-write register vertical redundancy error when the delay counter advances to 36. Even if the check character has bits, the RDD-36 pulse initiates the vertical redundancy check on the character in the read-write register.

Tape Read Operation Disconnect

The tape read operation can be terminated when the tape synchronizer processes the check character. Read disconnect delay pulses provide timings to check the LRCR and reset all circuits in the tape synchronizer. Because 729 and 7330 tape units have different characteristics, disconnect procedures for the two types of tape units differ; however, both procedures accomplish the same result.

729 DISCONNECT

At RDD-36 time, the go latch is reset to stop tape movement. The mechanical delay in stopping, however, allows sufficient time for the read operation to be completed.

The read disconnect delay counter runs throughout the check character cycle. The "RDD-128" pulse resets the read condition latch, causing the gate for the last stage of the final amplifiers to become inactive. At RDD-136 time, the LRCR is sampled for errors. All LRCR triggers should be off; if one or more LRCR triggers are on, indicating that bits have been picked up or dropped, the error latch is set.

The "RDD-144" pulse resets the tape in process latch and conditions "RDD-144 reset".

The off state of the tape in process latch allows the 1410 or 7010 channel committed to the tape read operation to disconnect.

The RDD-144 reset pulse turns off:

1. The load point latch.
2. The gate-on-final amplifiers latch.
3. The delay counter.
4. The check character latch.
5. The odd redundancy latch.
6. The read only latch.
7. The read disconnect delay latch.

When the read only latch is reset, "tape busy" drops freeing the tape synchronizer to control another tape operation. In 7040/7044 operation, the data channel that initiated the tape read operation is disconnected when "tape busy" drops.

7330 DISCONNECT

At RDD-110 time:

1. The read condition latch is reset.
2. The read disconnect delay latch is reset.
3. The delay counter is reset.
4. The LRCR is sampled for errors. All LRCR triggers should be off; if one or more LRCR triggers are on, indicating that bits have been picked up or dropped, the error latch is set.
5. The forward-stop delay latch is set.

The forward-stop delay latch conditions the delay counter for millisecond operation. Delay counter outputs combine with the output of the forward-stop delay latch providing forward-stop delay (FSD) timings.

The FSD-1 pulse (1414-1 and 2) or (FSD-2 pulse (1414-7) conditions "compute". "Compute" resets the tape in process latch allowing the 1410 or 7010 channel committed to the tape read operation to disconnect. No other tape operation requiring use of the tape synchronizer can be initiated, however, until "tape busy" drops.

At FSD-98 time, the RDD-144 reset line is forced up although the delay counter has only advanced to 98. The RDD-144 reset line turns off:

1. The gate-on-final amplifiers latch.
2. The forward-stop delay latch.
3. The check character latch.
4. The read only latch.
5. The odd redundancy latch.
6. The load point latch.
7. The delay counter.
8. The go latch.

When the read only latch is reset, "tape busy" drops, freeing the tape synchronizer to control another tape operation. In 7040/7044 operation, the data channel that initiated the tape read operation is disconnected when "tape busy" drops.

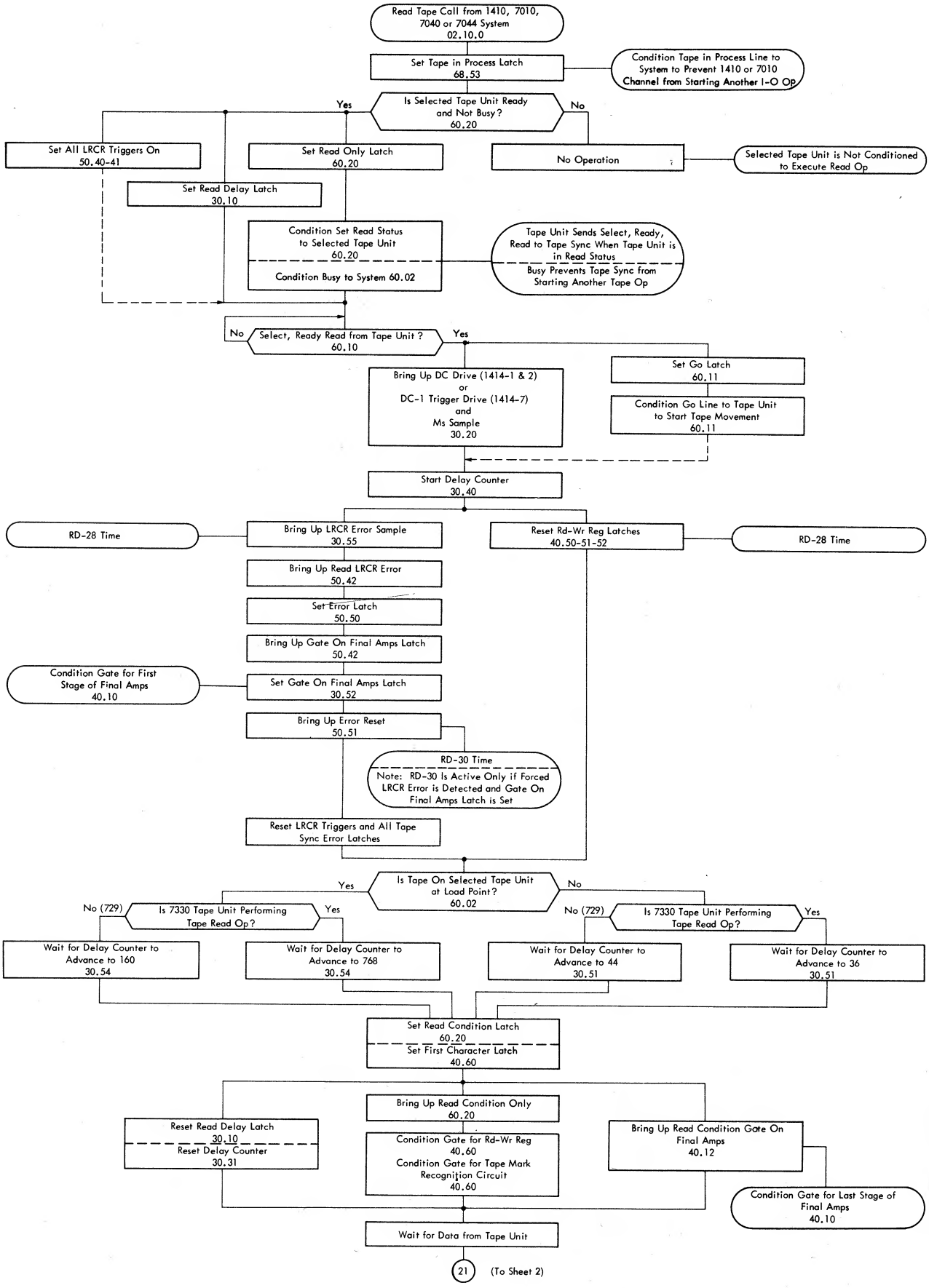


Figure 28. Tape Read Operation (Sheet 1 of 3)

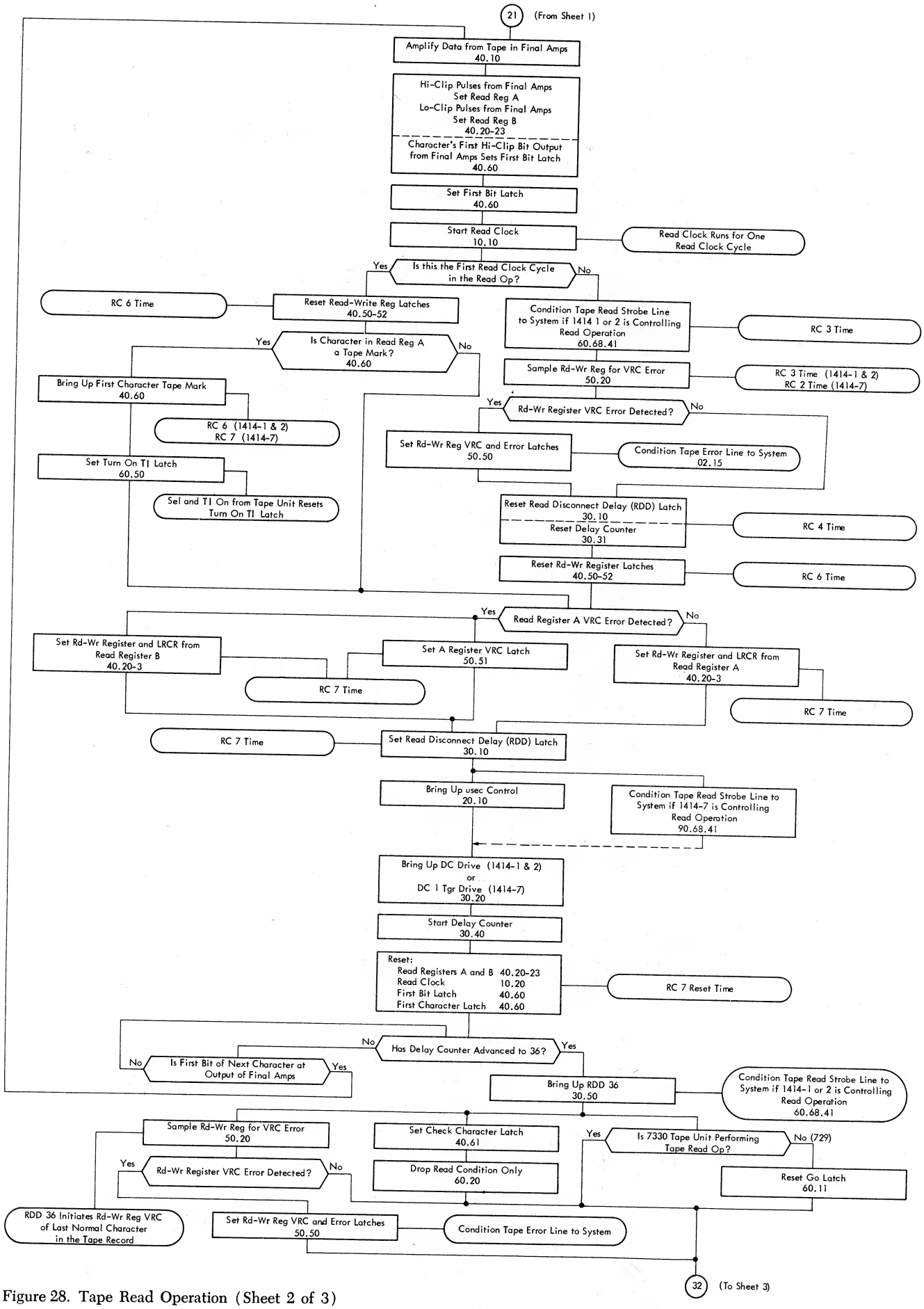


Figure 28. Tape Read Operation (Sheet 2 of 3)

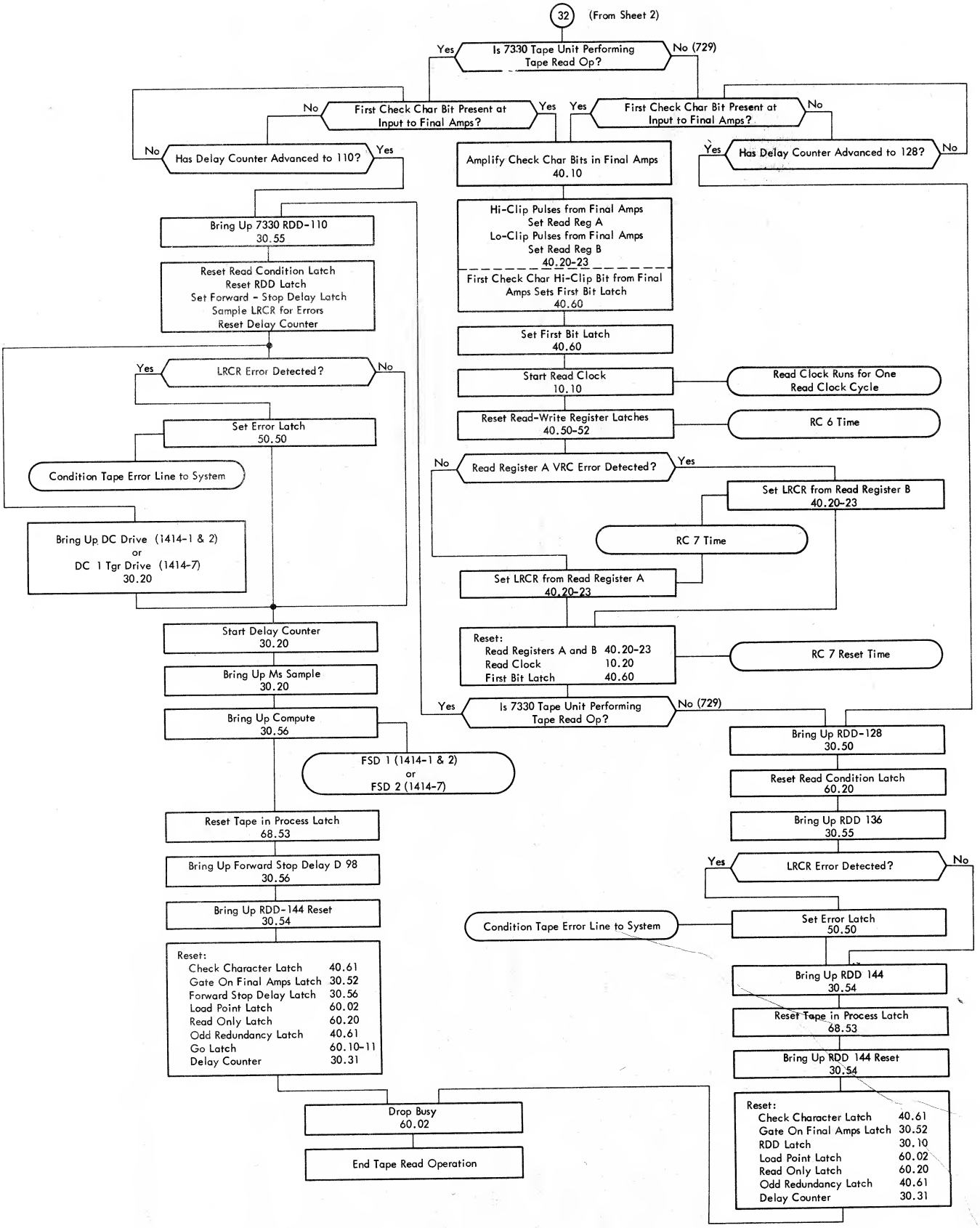


Figure 28. Tape Read Operation (Sheet 3 of 3)

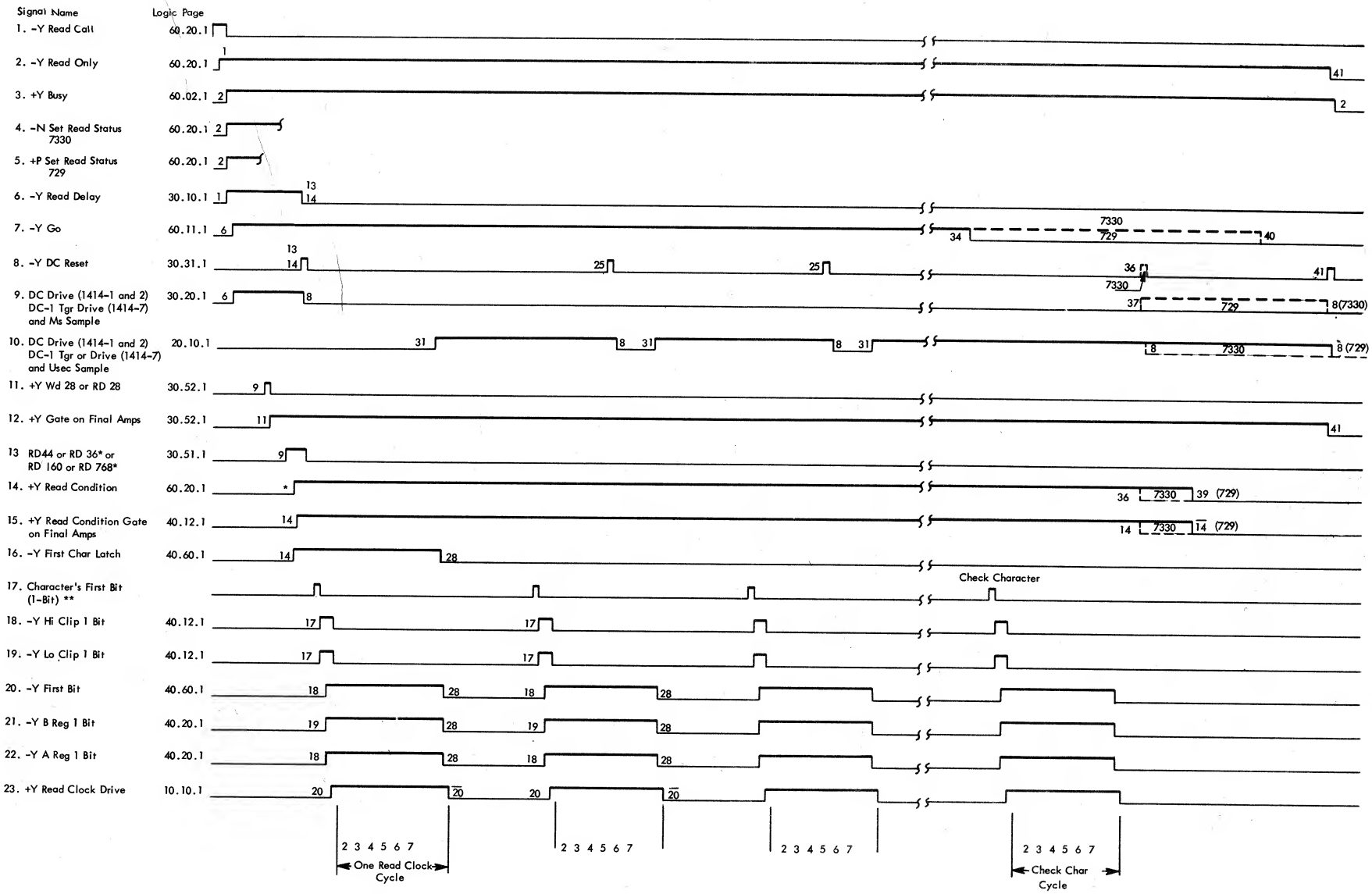
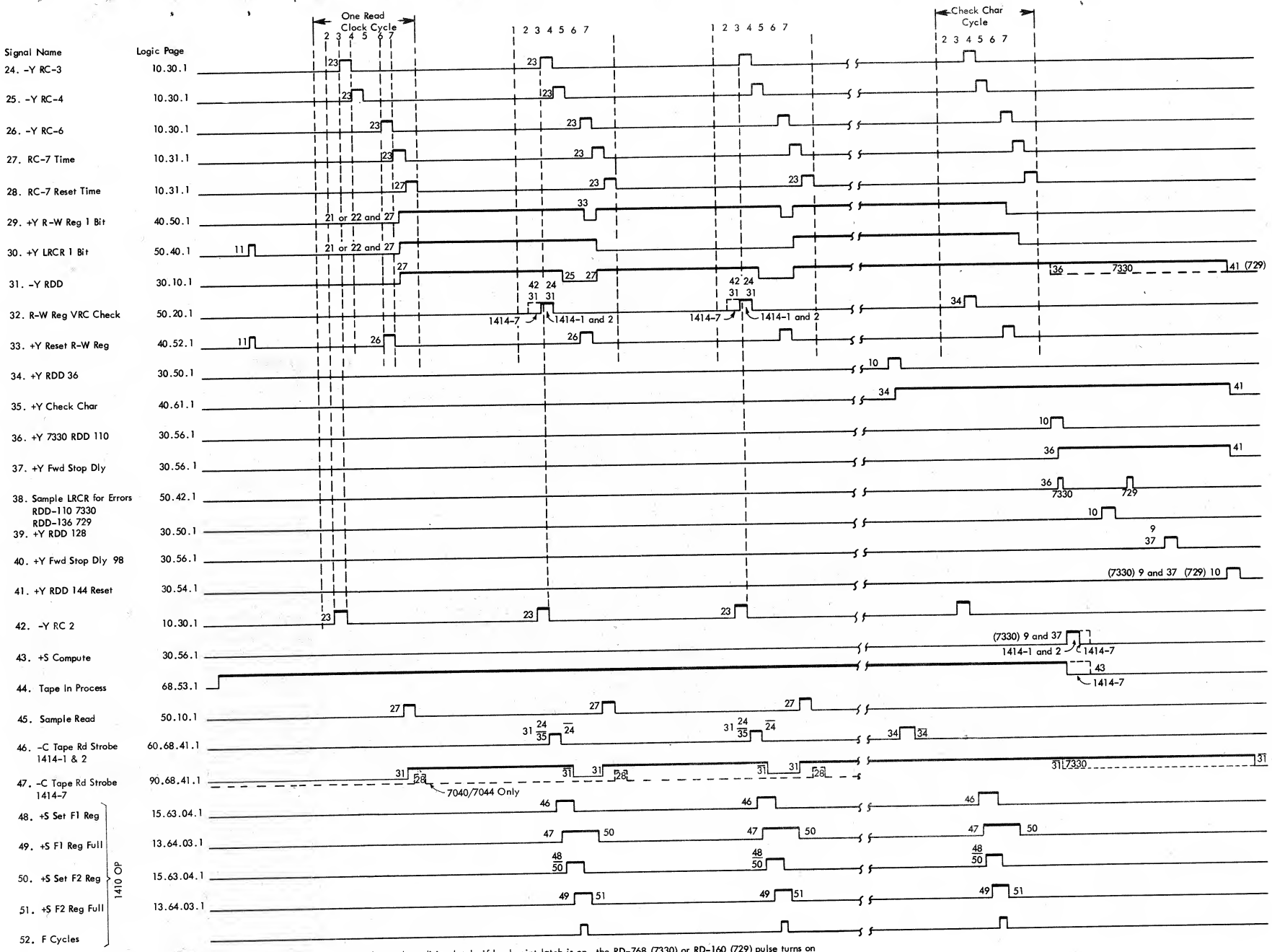


Figure 29. Tape Read Timings (Sheet 1 of 2)



* If load point latch is off, the RD-36 (7330) or RD-44 (729) pulse turns on the read condition latch; if load point latch is on, the RD-768 (7330) or RD-160 (729) pulse turns on the read condition latch

** The 1-bit line is typical of all data lines

Figure 29. Tape Read Timings (Sheet 2 of 2)

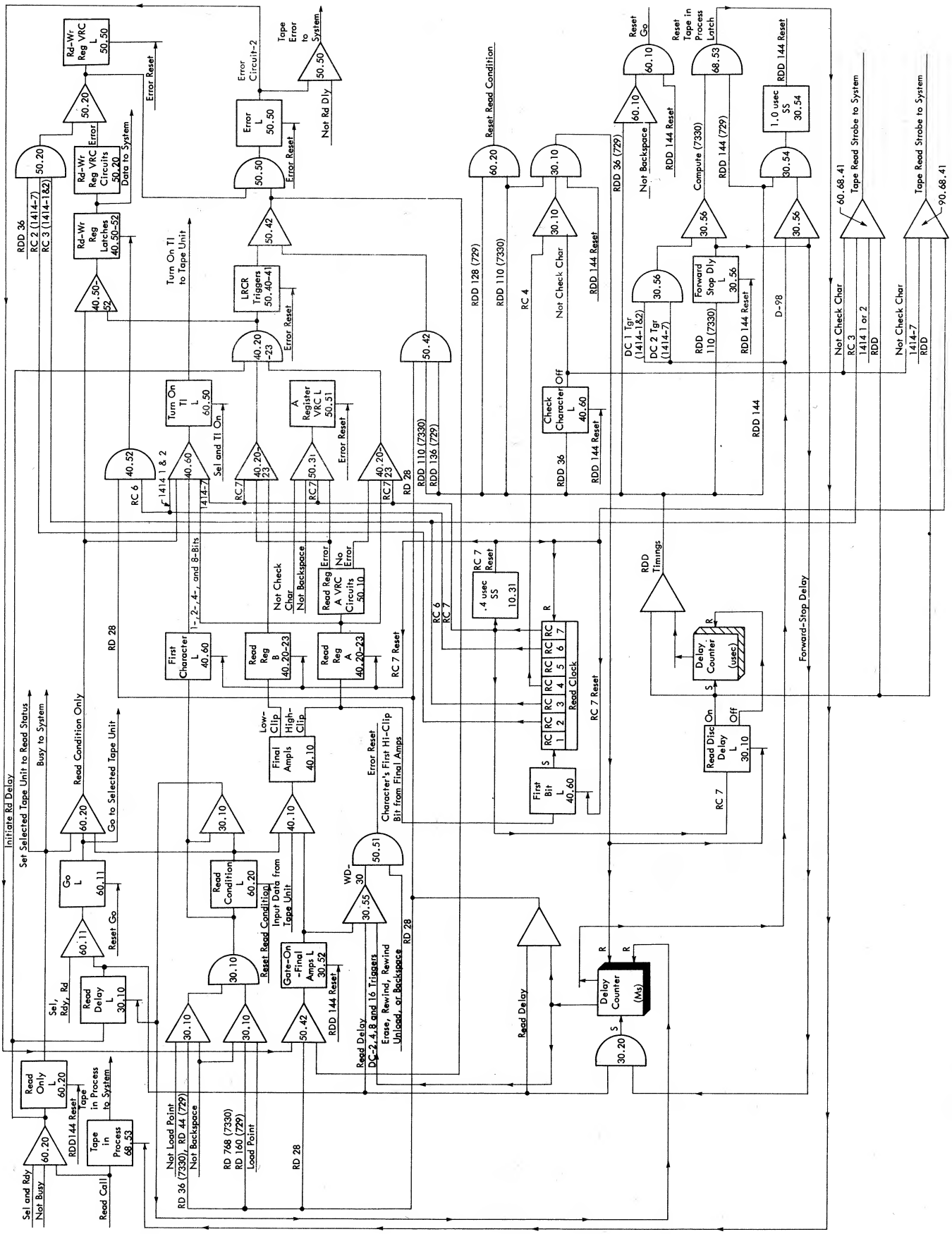


Figure 30. Read Circuits

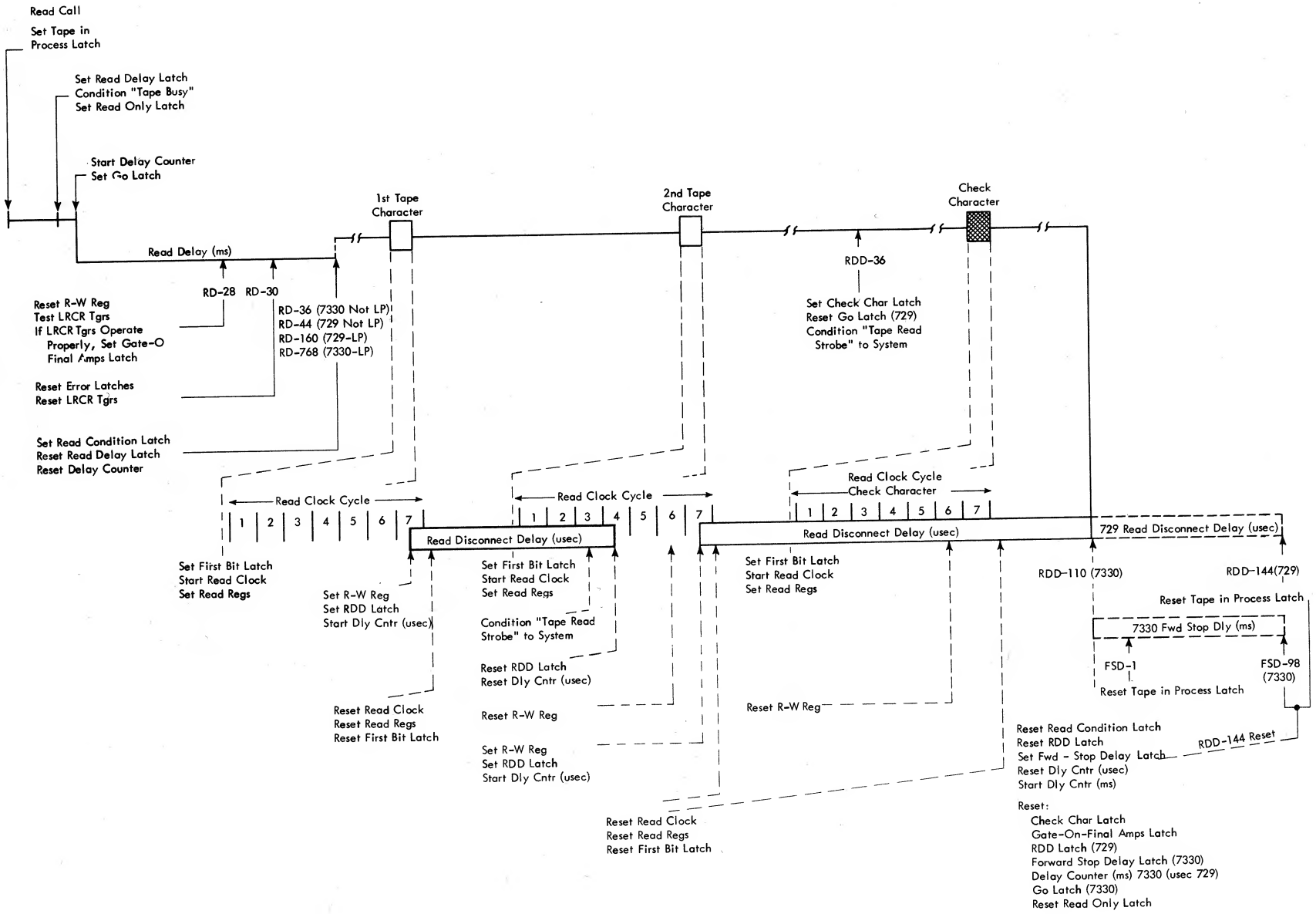


Figure 31. Simplified Read Operation Sequence

Tape Unit Control

In 1410/7010 operation, a tape unit control instruction, U (%Un) d, to the processing unit specifies one of five tape operations: erase, rewind, rewind unload, backspace, or write tape mark. The d-character in the instruction designates the specific operation to be performed. In 7040/7044 operation, a tape unit control instruction designates one or two of the five tape unit control operations. For example, the write end of file instruction causes the tape unit to erase a section of tape before writing the end of file (tape mark) character. This requires the tape synchronizer to execute two unit control operations. In all cases, however, execution of a tape unit control instruction requires no character transfers between the processing unit (1410/7010) or the data channel (7040/7044) and the selected tape unit.

Erase

In the erase operation, the tape unit that the erase instruction designates skips about 3¾ inches of tape before writing the next record.

7040/7044 OPERATION

Execution of the write blank tape instruction causes the data channel to send the erase call and write call signals to the tape synchronizer.

The erase call line:

1. Conditions "error reset," causing all error circuits in the tape synchronizer to turn off.
2. Sets the erase latch to simulate load point condition.

"Write call" conditions the tape synchronizer to perform a normal tape write operation. (See Tape Synchronization operations.) Because the erase latch is set, simulating load point condition, the tape unit erases approximately 3¾ inches of tape before the "WD-320" pulse (729) or "WD-1088" pulse (7330) turns on the write condition latch. The tape synchronizer sends "write condition" to the data channel, causing the channel to condition the computer reset to tape line. "Computer reset to tape" brings up "TAU reset" to reset all tape synchronizer circuits to their OFF states and disconnect the data channel from the write blank tape operation.

1410/7010 OPERATION

Execution of the U (%Un) E instruction causes the processing unit to send "erase call" to the tape synchronizer.

The erase call line:

1. Conditions "error reset," causing all error latches in the tape synchronizer to turn off.
2. Sets the erase latch to simulate load point condition.

Because the erase latch is set, the tape unit erases approximately 3¾ inches of tape before the WD-320 pulse (729) or WD-1088 pulse (7330) turns on the write condition latch in the next tape write operation. The tape synchronizer does not begin the write operation, however, until the processing unit decodes the M/L (%Un)(B)W instruction and conditions "write call". The erase latch is reset, and the erase operation is not performed if the system initiates a read, rewind, rewind unload, or backspace operation after the erase latch is set and before the write operation begins.

Rewind

Execution of the U (%Un) R (1410/7010) instruction or the rewind (7040/7044) instruction causes the system to send "rewind call" to the tape synchronizer. Because tape should never move backward beyond load point, no actions occur if the load point latch is set when the tape synchronizer receives "rewind call."

If tape on the selected tape unit is not at load point, "rewind call":

1. Brings up "error reset," causing all error latches in the tape synchronizer to turn off.
2. Sets the rewind latch.

The output of the rewind latch:

1. Conditions "tape busy." When "tape busy" is conditioned, the tape synchronizer cannot be designated to execute another tape operation, and the 7040/7044 data channel that issued the "rewind call" cannot communicate with any other I-O device.
2. Initiates the rewind operation on the selected tape unit.

The 7330 tape unit rewinds tape at low speed regardless of the amount of tape on the machine reel. When the selected tape unit begins the rewind operation, it conditions "select and rewind" to the tape synchronizer to reset the rewind latch. Tape synchronizer functions end and "tape busy" drops when the rewind latch is reset. The selected tape unit rewinds tape to load point without further control from the tape synchronizer.

Rewind Unload

Execution of the U (%Un) U (1410/7010) or the rewind unload (7040/7044) instruction causes the system to condition "rewind unload call" to the tape synchronizer. If tape is at load point when the tape synchronizer receives "rewind unload call," 729 tape units perform the unload actions in the operation; 7330 tape units "hang up" the channel. In both cases, tape is not moved backward beyond load point. If tape on the se-

lected tape unit is not at load point, "rewind unload call":

1. Brings up "error reset," causing all error latches in the tape synchronizer to turn off.
2. Sets the rewind unload latch.

The output of the rewind unload latch:

1. Conditions "tape busy." When "tape busy" is active, the tape synchronizer cannot be designated to execute another tape operation, and the 7040/7044 data channel that issued "rewind unload call" cannot communicate with any other I-O device.
2. Initiates the rewind unload operation on the selected tape unit.

The 7330 tape unit unloads and rewinds tape at high speed. When the selected tape unit begins the rewind unload operation, the select and rewind line is sent to the tape synchronizer to reset the rewind unload latch. Tape synchronizer functions end and "tape busy" drops when the rewind latch is reset. The selected tape unit completes the operation without further control from the tape synchronizer.

Write Tape Mark

In 7040/7044 operation, execution of the write end of file instruction causes the designated data channel to condition "erase call," then "write tape mark call" to the tape synchronizer. The erase call line:

1. Conditions "error reset," causing all error latches in the tape synchronizer to turn off.
2. Sets the erase latch to simulate load point condition.

In 1410/7010 operation, execution of the U (%Un)M instruction causes the processing unit to condition "write tape mark call" to the tape synchronizer; "erase call" is not issued.

The write tape mark call line turns on the tape in process, write, write delay, and disconnect latches. The tape synchronizer is conditioned to perform a normal tape write operation; because the disconnect latch is set, the write operation is limited to one cycle. (See Tape Synchronizer Operations.)

Regardless of the position of tape in 7040/7044 operation, the erase latch causes the tape unit to erase about 3¾ inches of tape before the WD-320 pulse (729) or WD-1088 pulse (7330) sets the write condition latch.

In 1410/7010 operation, the write condition latch is set:

1. When the delay counter advances to 50 (729) or to 72 (7330) if tape on the selected tape unit is not at load point when the write tape mark operation begins.
2. When the delay counter advances to 320 (729) or 1088 (7330) if tape is at load point when the write tape mark operation begins.

The WC-1 pulse resets the read-write register. The output of the write tape mark latch blocks the input gate for the read-write register and automatically sets the read-write register 8-, 4-, 2-, and 1-bit data latches at WC-2 time. Read-write register data are not transferred to the system in the write tape mark operation.

All tape synchronizers condition the write pulse for 7330 tape units from WC-4 to WC-8 time. The trailing edge of the write pulse causes the selected 7330 tape unit to write the tape mark.

At WC-9 time (1414-1 and 2) or WC-12 time (1414-7), the tape synchronizer sends "write pulse" to the 729 tape unit. The leading edge of "write pulse" causes the selected 729 to write the tape mark.

The write disconnect delay latch is set at WC-14 time to begin the disconnect operation. Because only one character was written, the 8-, 4-, 2-, and 1-bit write triggers in the tape unit are on. When the write triggers reset, the tape unit writes an 8-, 4-, 2-, and 1-bit check character.

The write tape mark operation ends in the same manner that a normal tape write operation terminates. (See Tape Synchronizer Operations.)

Backspace

In a backspace operation, the tape unit moves tape backward through one tape record to the first interrecord gap or to the gap between the load point reflective spot and the first record. Although characters are read and transferred to the tape synchronizer as tape moves past the read head on the tape unit, the tape synchronizer does not check the data. No characters are transferred between the system and the tape synchronizer. Figures 32, 33, and 34 show detailed tape synchronizer actions in the execution of the backspace operation.

PRELIMINARY CONDITIONS

Execution of the U(%Un)B (1410) or the backspace record (7040/7044) instruction causes the system to condition "backspace call" to the tape synchronizer. Because tape should never move backward beyond load point, no actions occur if the load point latch is set when the tape synchronizer receives "backspace call." If tape on the selected tape unit is not at load point, "backspace call" sets the backspace latch.

The output of the backspace latch:

1. Brings up "error reset," causing all error latches in the tape synchronizer to turn off.
2. Conditions "tape busy." When "tape busy" is conditioned, the tape synchronizer cannot be designated to execute another tape operation, and the 7040/7044 data channel that issued "backspace call" cannot communicate with any other I-O device.

3. Conditions the delay counter for operation in the millisecond mode.

The tape unit must be in read status to move tape backward. If the tape unit is in write status, tape moves forward to insure that noise deposited on tape during the status change will be erased in a subsequent write operation. If the tape unit is in read status when the system conditions "backspace call," the tape unit does not move tape forward.

If the tape unit is in write status when the delay counter advances to 1 (1414-1 and 2) or 2 (1414-7), the go latch is set, causing the tape unit to move tape forward. When the delay counter advances to 50 (729) or 128 (7330), the go latch is reset; tape movement stops after normal mechanical delays.

The backward latch turns on:

1. When the delay counter steps to 96 if a 729 tape unit performs the backspace operation.

2. When the delay counter steps to 128 if a 7330 tape unit in write status is selected to perform the backspace operation.

3. Immediately if a 7330 tape unit in read status performs the backspace operation. The output of the backward latch sets the selected tape unit to backward status and, if the tape unit is in write status, to read status. If a 7330 tape unit in write status is selected to perform the backspace operation, the delay counter is reset when the counter advances to 128, but because the backspace latch is set, the delay counter starts again.

The tape unit conditions "select, ready, and read" to the tape synchronizer when the tape unit is in read status. The delay counter output "D-160" (729) or "D-2048" (7330):

1. Sets the go latch, and because the tape unit is in backward status, tape moves backward. The delay between the times that the backward and go latches are set allows the tape unit sufficient time to transfer to backward status.

2. Sets the gate-on-final amplifiers latch to condition the gate for the first stage of the final amplifiers.

The delay counter output "D-180" (729) or "D-64"* (7330) sets the read condition latch and resets the delay counter. The read condition latch gates the last stage of the final amplifiers and blocks the output of the backspace latch from starting the delay counter. Between the times that the go and read condition latches are set, tape reaches proper operating speed.

CHARACTER CYCLES

Each character from tape is set in the final amplifiers in the tape synchronizer. The first high-clip bit from the final amplifiers sets the first bit latch. The first bit latch unclamps read clock oscillators and allows the read clock to run for one cycle. The low-clip output of the final amplifiers sets read register B; the high-clip output sets read register A. The read registers and the first bit latch are reset at the end of the cycle. The next character from tape initiates the same operation. This action occurs until the beginning of the record is reached.

The "RC-7" pulse sets the read disconnect delay latch, causing the delay counter to advance in the millisecond mode. If the delay counter does not advance to 16 (729) or 78 (7330) before the read clock advances to 4 in the subsequent read clock cycle, the read disconnect delay latch and the delay counter are reset. If, however, the delay counter advances to 16 (729) or 78 (7330) before the read disconnect latch and the delay counter are reset, the disconnect operation begins. However, the first bit of the following character from tape should arrive soon enough to advance the read clock to 4 before the delay counter steps far enough to initiate the disconnect operation. The inter-record gap separates the first character of the record and the check character of the previous record. Therefore, when the beginning of the record is reached, the delay counter steps to 16 (729) or 78 (7330) before the next character is read from tape.

DISCONNECT

In 7330 operation, the read condition, go, and backward latches are reset when the delay counter advances to 78. In 729 operation, the read condition latch is reset when the delay counter advances to 16. The RDD-22 pulse (729 IV or VI) or RDD-38 pulse (729 II or V) resets the go latch, and the RDD-64 pulse resets the backward latch.

When the read condition latch is reset, the gate for the last stage of the final amplifiers drops.

When the go latch turns off, normal mechanical delay insures that the tape unit will stop tape with the read-write head to the left of the record. The next read or write operation will not miss the first character of the record.

When the backward latch resets, the tape unit is automatically set to forward status.

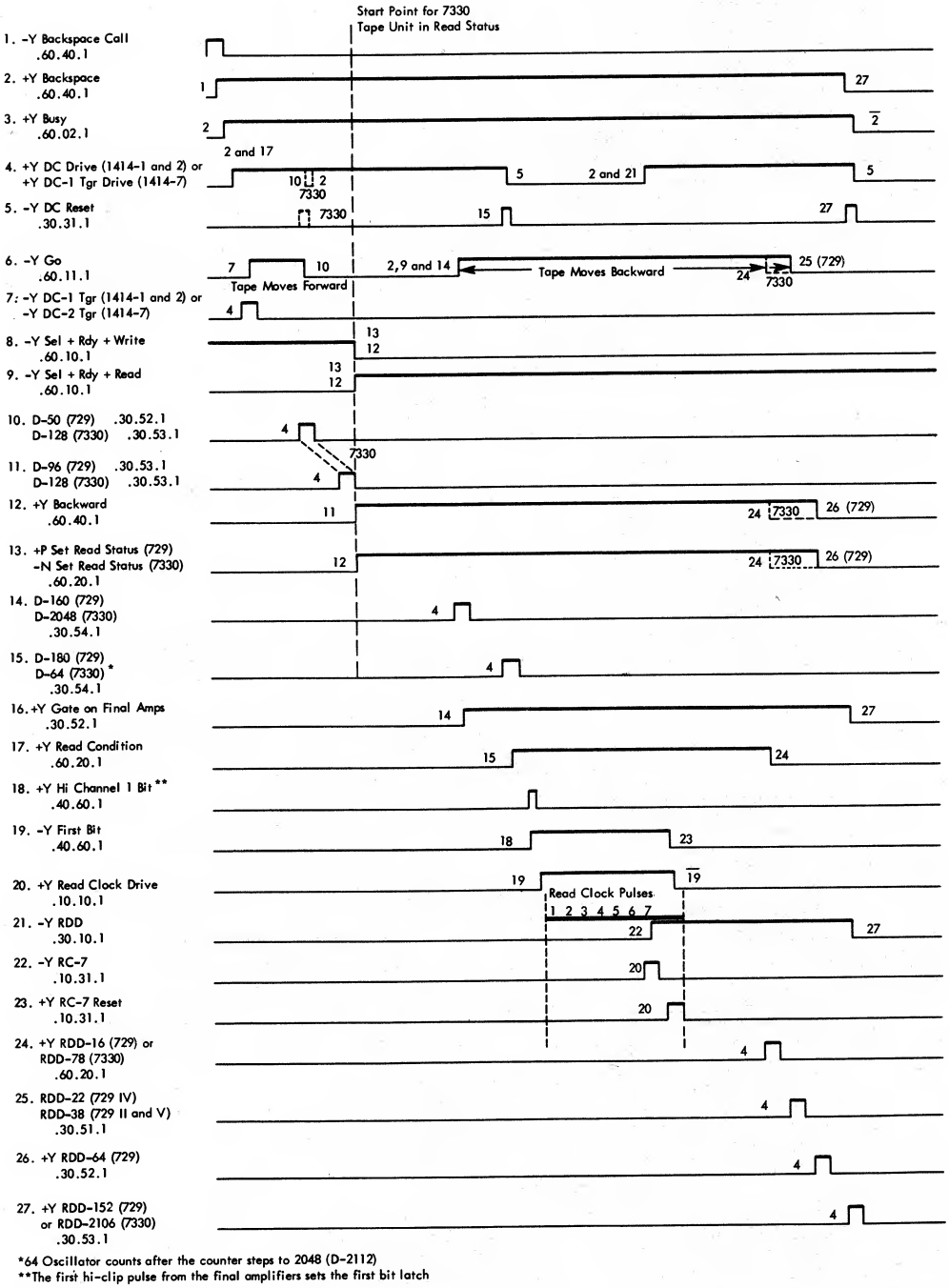
The RDD-152 pulse (729) or RDD-2106 pulse (7330):

1. Resets the backspace latch, causing the tape busy line to the system to drop.

2. Conditions RDD-144 reset."

The RDD-144 reset line turns off the read disconnect delay latch, the gate-on-final amplifiers latch, and the delay counter.

*The "D-64" output of the delay counter is active after the delay counter has advanced 64 counts beyond 2048. Theoretically, this "D-64" output is the D-2112 output.



*64 Oscillator counts after the counter steps to 2048 (D-2112)
**The first hi-clip pulse from the final amplifiers sets the first bit latch

Figure 32. Backspace Timings

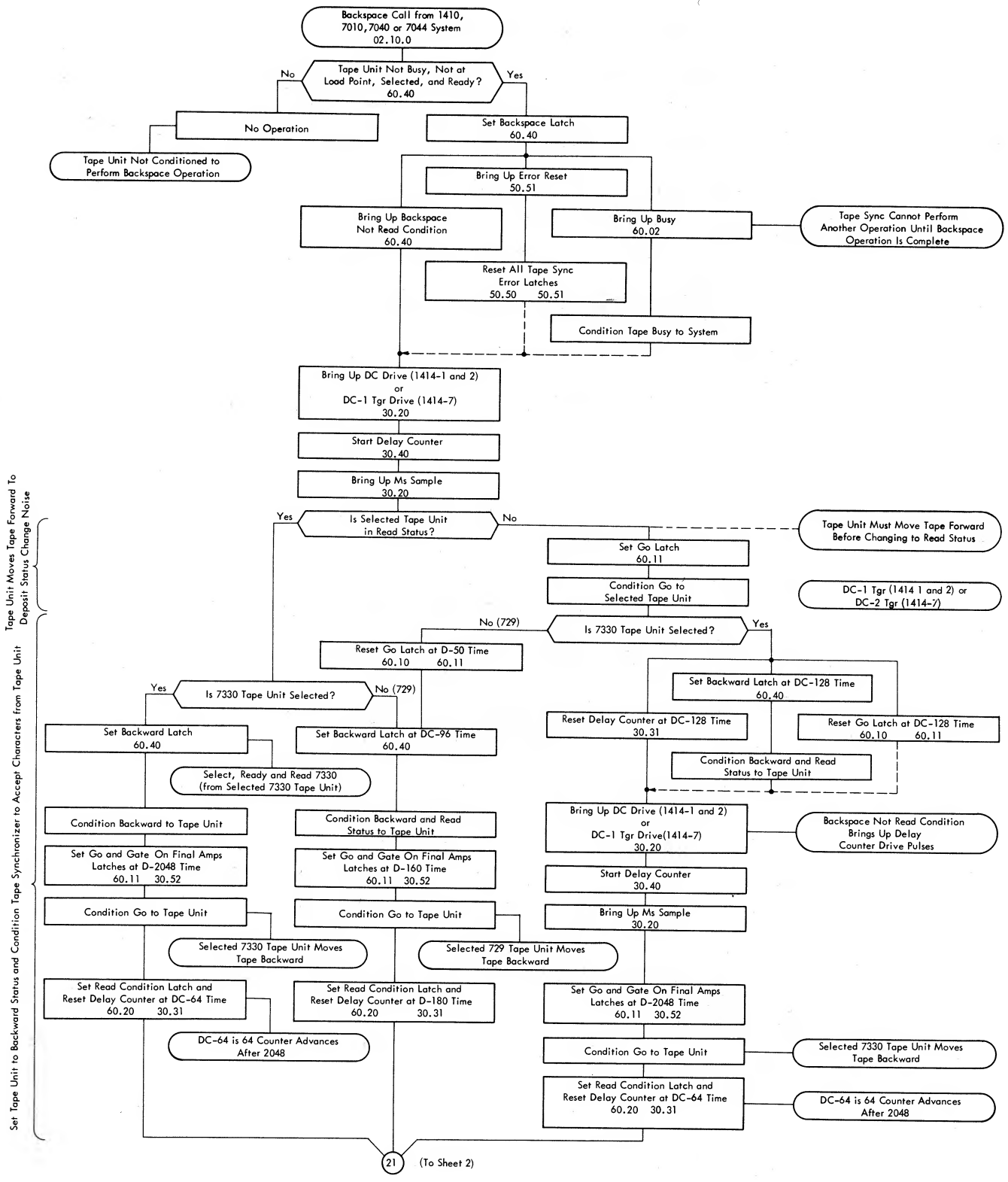


Figure 33. Backspace Operation (Sheet 1 of 2)

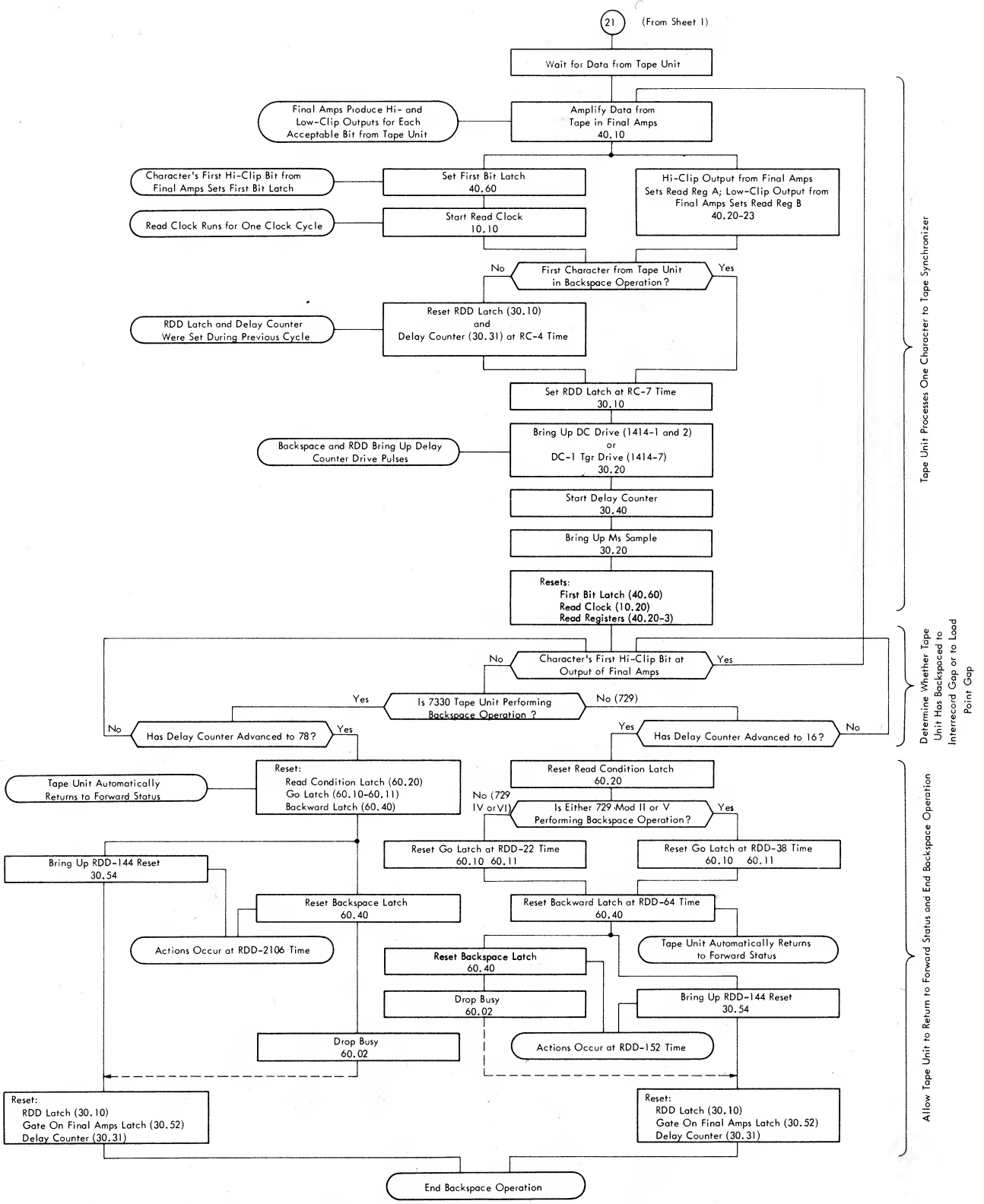


Figure 33. Backspace Operation (Sheet 2 of 2)

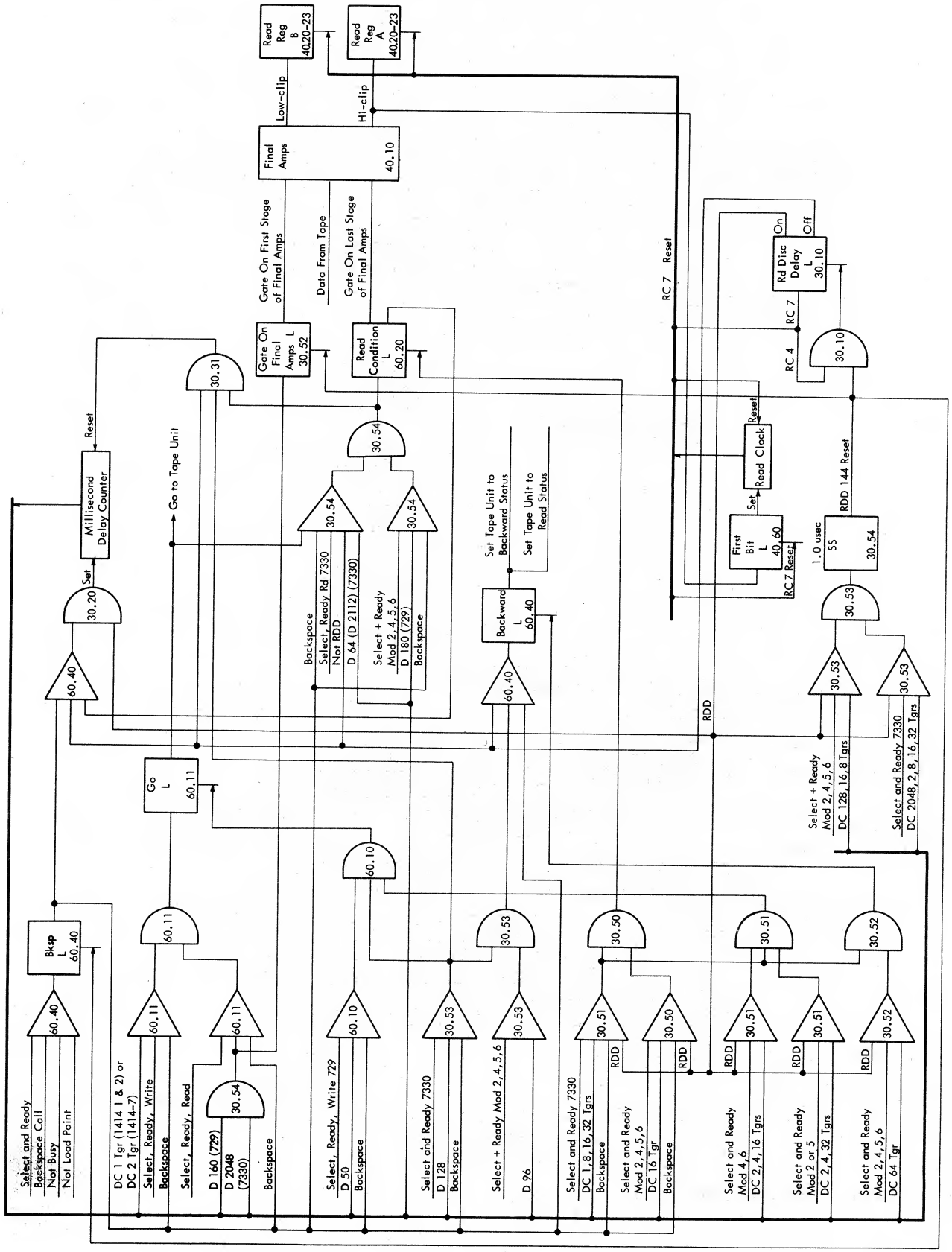


Figure 34. Backspace Circuits

Binary triggers can be connected in such a manner that their on and off states represent a numeric value. This type of configuration is called a binary counter. Each trigger in the arrangement represents a stage in the counter; therefore, a four-stage binary counter consists of four binary triggers tied in a counter configuration.

The counter configuration can be constructed in several ways. In 1414-1, 2, and 7 operation, however, drive pulses from a selected oscillator and/or outputs from stages in the counter condition the ac gate, set, and reset pins on all triggers in the binary counter.

To illustrate the general operation of a binary counter, assume that four binary triggers, labeled 1, 2, 4, and 8, are connected in a counter configuration and that an oscillator drives the four-stage counter. The first oscillator pulse to the counter sets trigger 1; the counter indicates 1. The second oscillator pulse resets trigger 1 and sets trigger 2; the counter indicates 2. The third oscillator pulse sets trigger 1; the counter indicates 3 (triggers 1 and 2 are on). The fourth oscillator pulse resets triggers 1 and 2 and sets trigger 4; the counter indicates 4. The sixteenth oscillator pulse resets triggers 1, 2, 4, and 8; the counter indicates 16 or 0, and one counter cycle is complete. Each oscillator pulse advances the counter one step and alternately sets and resets trigger 1. Every second oscillator pulse alternately sets and resets trigger 2. Every fourth pulse sets or resets trigger 4; every eighth pulse sets or resets trigger 8.

The binary counter does not have to count to the maximum point. The dc reset line, common to each stage of the counter, can be conditioned to shorten the counter cycle or to terminate the count.

In 1414-1 and 2 operation, selected oscillator pulses:

1. Drive triggers in the binary counters in parallel (i. e., triggers are set and reset in one operation).
2. Gate output timings from the delay counters.

In 1414-7 operation, oscillator pulses drive only the first stages in binary counters. The first stages drive the remaining triggers in the counters in parallel and gate output timings from the respective counters. Timings are shifted by half an oscillator cycle in 1414-7 operation relative to the equivalent timings in 1414-1 and 2 operation.

Three binary counters provide the timings required in tape synchronizers. The counter circuits are called the delay counter, read clock, and write clock. The oscillator selected to drive each counter determines the circuit's output frequency. Figure 35 lists oscillators in the tape synchronizer. Figure 36, 37, 38, and 39 list timings and clock pulses required to control tape unit operations.

Delay Counter

Delay counters in tape synchronizers that control only 729 tape units are ten-stage binary counters; triggers are labeled in binary sequence from DC-1 through DC-512. Delay counters in tape synchronizers that control 7330 tape units are twelve-stage binary counters; triggers are labeled in binary sequence from DC-1 through DC-2048.

The selected tape unit, the density at which the tape unit is operating, and the phase of the operation being executed designate one of nine (1414-1) or ten (1414-7) crystal oscillators to drive the delay counter. The selected oscillator determines whether the frequency of the output timings are in the millisecond or microsecond range. When the counter advances to the selected point, the dc reset line to each trigger in the counter is conditioned, and oscillator drive pulses to the counter are blocked, terminating the operation.

Delay counter outputs combine with outputs from the read and write delay latches to produce read and write delay timings (RD and WD). Read and write disconnect delay latches outputs AND with delay counter outputs forming read and write disconnect delay signals (RDD and WDD).

Read Clock

The read clock, a four-stage binary counter, supplies timings that the tape synchronizer requires to process characters from the tape unit. The selected tape unit, the density at which the tape unit is operating, and the status of the check character latch designate one of six (1414-1) or seven (1414-7) clamped oscillators to supply drive pulses to the read clock (Figures 40 and 41).

In the read check of a tape write operation, the first bit of a character detected at the output of the final amplifiers sets the first bit latch. In a tape read operation, the first high-clip bit detected at the output of the final amplifiers sets the first bit latch. The ON output of the first bit latch unclamps the read clock oscil-

Oscillator	Tape	Tape Unit	Frequency Accuracy (%)	Function
6.67 KC	Crystal	729 II and V	±1	Delay Counter Millisecond Control
10 KC	Crystal	729 IV, VI, and 7330	±1	Delay Counter Millisecond Control
115 KC	Crystal	7330	±1	Delay Counter Microsecond Control and Write Clock Drive (Low Density)
115 KC	Clamped	7330	±5	Read Clock Drive (Low Density)
240 KC	Crystal	729 II and V	±1	Delay Counter Microsecond Control and Write Clock Drive (200 cpi)
240 KC	Clamped	729 II and V	±5	Read Clock Drive (200 cpi)
320 KC	Crystal	7330	±1	Delay Counter Microsecond Control and Write Clock Drive (Hi Density)
320 KC	Clamped	7330	±5	Read Clock Drive (Hi Density)
360 KC	Crystal	729 IV and VI	±1	Delay Counter Microsecond Control and Write Clock Drive (200 cpi)
360 KC	Clamped	729 IV and VI	±5	Read Clock Drive (200 cpi)
667 KC	Crystal	729 II and V	±1	Delay Counter Microsecond Control and Write Clock Drive (555.5 cpi)
667 KC	Clamped	729 II and V*	±5	Read Clock Drive (555.5 cpi)
960 KC	Crystal	729 V	±1	Delay Counter Microsecond Control and Write Clock Drive (800 cpi)
1 MC	Crystal	729 IV and VI	±1	Delay Counter Microsecond Control and Write Clock Drive (555.5 cpi)
1 MC	Clamped	729 IV, V, and VI	±5	Read Clock Drive (729 IV and VI at 555.5 cpi and 729 V at 800 cpi)
1.44 MC**	Crystal	729 VI	±1	Delay Counter Microsecond Control and Write Clock Drive (800 cpi)
1.66 MC**	Clamped	729 VI	±5	Read Clock Drive (800 cpi)

* to prevent skew errors, the 729 V, uses the 667 KC clamped oscillator to read check characters when operating at 800 cpi.
** 1414-7 only

Figure 35. Tape Synchronizer Oscillators

lators, allowing the selected oscillator to supply drive pulses to the clock. In 1414-7 operation, the 360-kc oscillator drives the read clock when the tape synchronizer processes the check character. When the 729 v tape unit executes the tape operation, the 1414-1 tape synchronizer unconditionally selects the 667-kc oscillator to drive the read clock to process the check character.

The read clock cycle in the read check of a tape write operation is longer than the cycle in a tape read operation. In neither case, however, does the four-stage binary counter that makes up the clock advance to its maximum point. In a tape write operation, the read clock is reset at the end of read clock-10 (RC-10) time (when the delay counter advances to 11). In a tape read operation, the clock is reset at the end of RC-7 time (when the delay counter advances to 8).

The line that resets the clock also resets the first bit latch, clamping the read clock oscillators. The next read clock cycle begins when the tape unit transfers the next character to the tape synchronizer.

Write Clock

The write clock, a four-stage binary counter, supplies timings that the tape synchronizer requires to process characters from the processing unit to the tape unit. The selected tape unit and the density at which the tape unit is operating designate one of seven (1414-1) or eight (1414-7) crystal oscillators to supply drive pulses to the write clock (Figure 42). However, the clock can be driven only when the write condition latch is set, or the fourth stage (write clock-8 trigger) is on.

When the write condition latch is set, the selected oscillator continuously supplies drive pulses to the

Output	Tape Synchronizer	200 cpi			556 cpi			800 cpi	
		7330	729 II or V	729 IV or VI*	7330	729 II or V	729 IV or VI*	729 V	729 VI*
RC-2	1414-7	22.05	10.72	7.25	8.11	4.05	2.8	2.8	1.86
RC-3	1414-1	26.4	12.8	8.6	9.7	4.8	3.3	3.3	
RC-4	1414-1	35.1	16.9	11.4	12.8	6.3	4.3	4.3	
RC-4	1414-7	39.45	19.05	12.80	14.36	7.05	4.8	4.8	3.11
RC-5 (Write)	1414-1	43.8	21.1	14.2	15.9	7.8	5.3	5.3	
RC-6	1414-1	48.1	23.2	15.6	17.5	8.5	5.8	5.8	
RC-6	1414-7	56.8	27.40	18.36	20.60	10.05	6.8	6.8	4.36
RC-6 Delay	1414-7	61.20	29.47	19.74	22.15	10.80	7.3	7.3	
RC-7 (Read)	1414-1	61.2	29.5	19.7	22.2	10.8	7.3	7.3	
RC-7 (Set)	1414-7	65.65	31.65	21.23	23.82	11.65	7.9	7.9	5.09
RC-7 Reset (Read)	1414-1	65.6	31.7	21.2	23.8	11.6	7.9	7.9	
RC-7 Reset (Read)	1414-7	66.15	32.15	21.73	24.32	12.15	8.4	8.4	5.59
RC-10 Reset (Write)	1414-1	91.7	44.2	29.6	33.2	16.1	10.9	10.9	
RC-10 Reset (Write)	1414-7	91.7	44.2	29.6	33.2	16.1	10.9	10.9	6.96

*1414-7 only
**all read clock timings are in microseconds and are measured with respect to the rise of the first bit line. Tolerances are ±5%.

Figure 36. Read Clock Outputs

write clock, causing the clock to cycle repetitively (i. e., after the four-stage delay counter steps to 15 and is reset, the next cycle begins immediately). In the last clock cycle, the write condition latch is reset when the clock advances to 14. The write clock-8 trigger gates drive pulses from the selected oscillator to the clock, allowing the clock to complete the cycle. The write clock does not run again in the operation.

Output	Tape Synchronizer	200 cpi			555.5 cpi			800 cpi	
		7330	729 II or V	729 IV or VI*	7330	729 II or V	729 IV or VI*	729 V	729 VI*
WC-1	1414-1	Ref	Ref	Ref	Ref	Ref	Ref	Ref	Ref
WC-1	1414-7	Ref	Ref	Ref	Ref	Ref	Ref	Ref	Ref
WC-2	1414-1	8.70	4.17	2.78	3.12	1.50	1.00	1.04	
WC-2	1414-7	17.40	8.34	5.56	6.24	3.00	2.00	2.08	1.39
WC-4	1414-1	26.09	12.50	8.34	9.38	4.50	3.00	3.12	
WC-4	1414-7	34.80	16.68	11.12	12.48	6.00	4.00	4.16	2.78
WC-6	1414-7	52.20	25.02	16.68	18.73	9.00	6.00	6.24	4.17
WC-9	1414-1	65.21	31.25	20.84	23.44	11.24	7.50	7.81	
WC-12	1414-7	95.70	45.87	30.58	34.40	16.50	11.00	11.44	7.65
WC-14	1414-1	113.05	54.17	36.11	40.63	19.47	13.00	13.54	
WC-14	1414-7	121.80	58.38	38.92	43.68	21.00	14.00	14.56	9.73
WC-1	1414-1	139.14	66.67	44.45	50.00	24.00	16.00	16.67	
WC-1	1414-7	139.14	66.67	44.45	50.00	24.00	16.00	16.66	11.1
WC-4 to WC-8	1414-1	21.74			7.81				
WC-4 to WC-8	1414-7	26.10			9.36				

*1414-7 only
**all write clock timings are in microseconds and are measured with respect to the turn-on of the WC-1 pulse. Tolerances are ± 1%

Figure 37. Write Clock Outputs

Output	Tape Synchronizer	200 cpi			556 cpi			800 cpi	
		7330	729 II or V	729 IV or VI*	7330	729 II or V	729 IV or VI*	729 V	729 VI*
RDD-36	1414-1	313.0	150.0	100.0	112.5	54.0	36.0	37.5	
RDD-36	1414-7	317.4	152.1	101.4	114.1	54.8	36.5	38.1	25.4
RDD-128	1414-1	-----	533.3	355.5	-----	192.0	128.0	133.3	
RDD-128	1414-7	-----	536.0	357.0	-----	192.8	128.5	133.9	89.2
RDD-136 or 110	1414-1	956.6	566.7	377.7	343.8	204.0	136.0	141.7	
RDD-136 or 110	1414-7	961.0	568.8	379.1	345.3	204.8	136.5	142.2	94.8
RDD-144	1414-1	-----	600.0	400.0	-----	216.0	144.0	150.0	
RDD-144	1414-7	-----	602.1	401.4	-----	216.8	144.5	150.5	100.3
WDD-60	1414-1	521.7	250.0	166.7	187.5	90.0	60.0	62.5	
WDD-60	1414-7	526.0	252.1	168.1	189.1	90.8	60.5	63.0	42.0

*1414-7 only
**Tolerance on all other delay counter microsecond timings except RDD-36 is ± 1%; RDD-36 tolerance is ± 2%

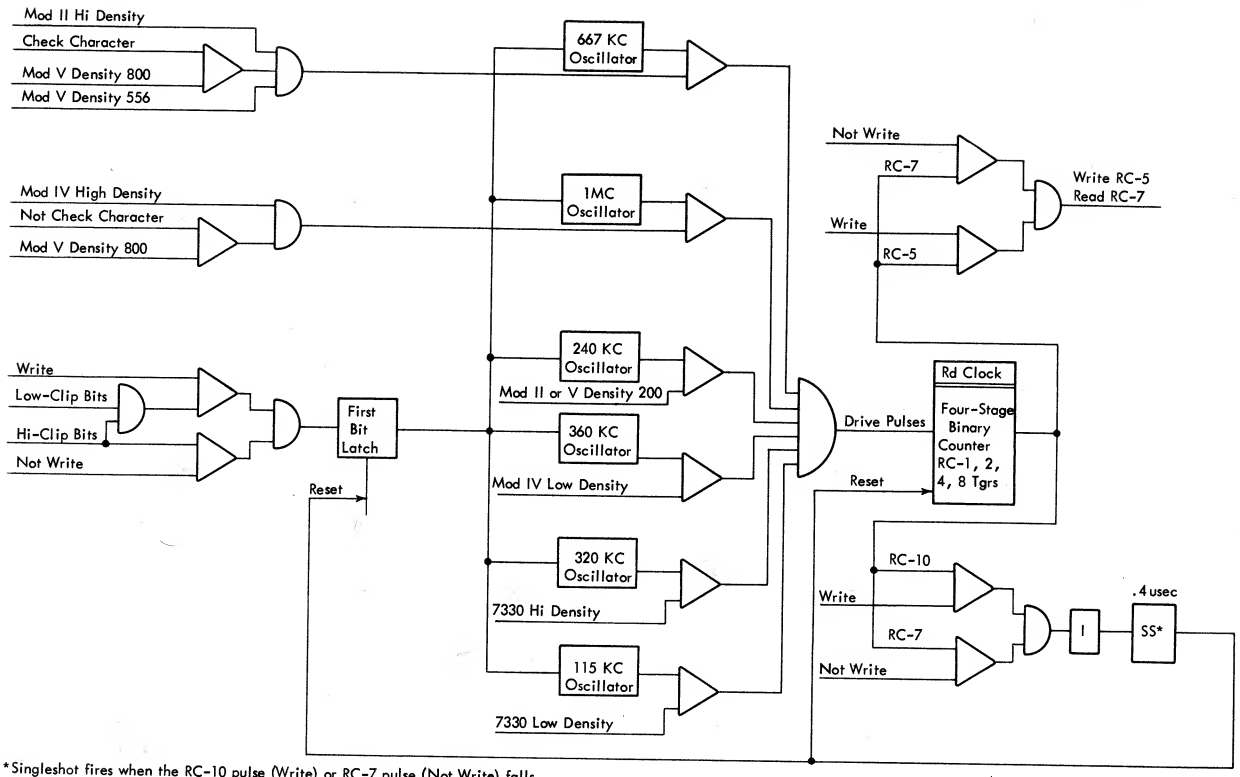
Figure 38. Delay Counter — Microsecond Outputs

	Tape Synchronizer	7330	729 II or V	729 IV or VI*	Tolerance
RDD-16 or 78	1414-1	7.8 ±3%	2.4 ±5%	1.6 ±5%	
RDD-16 or 78	1414-7	7.85 ±3%	2.48 ±5%	1.65 ±5%	
End Bkwd Stop Delay	1414-1	7.8	5.7	22.0	±3%
End Bkwd Stop Delay	1414-7	7.85	5.78	22.05	±3%
RDD-64 or 78	1414-1	7.8	9.6	6.4	±2%
RDD-64 or 78	1414-7	7.85	9.68	6.45	±2%
RDD-152 or 2106	1414-1	210.6	22.8	15.2	±1%
RDD-152 or 2106	1414-7	210.65	22.88	15.25	±1%
WDD-20	1414-1	2.0	3.0	2.0	±5%
WDD-20	1414-7	2.05	3.08	2.05	±5%
RD-44 or 36	1414-1	3.6	6.6	4.4	±2%
RD-44 or 36	1414-7	3.65	6.68	4.45	±2%
RD-160 or 768	1414-1	76.8	24.0	16.0	±1%
RD-160 or 768	1414-7	76.85	24.08	16.05	±1%
WD-28 or RD-28	1414-1	2.8	4.2	2.8	±2%
WD-28 or RD-28	1414-7	2.85	4.28	2.85	±2%
WD-30 or RD-30	1414-7	3.0	4.5	3.0	±2%
WD-32	1414-1	-----	4.8	3.2	±2%
WD-32	1414-7	-----	4.88	3.25	±2%
WD-96	1414-1	-----	14.4	9.6	±2%
WD-96	1414-7	-----	14.48	9.65	±2%
WD-320 or 1088	1414-1	108.8	48.0	32.0	±1%
WD-320 or 1088	1414-7	108.85	48.08	32.05	±1%
D-50 or WD-72	1414-1	7.2	7.5	5.0	±2%
D-50 or WD-72	1414-7	7.25	7.58	5.05	±2%
D-96 or 128	1414-1	12.8	14.4	9.6	±1%
D-96 or 128	1414-7	12.85	14.48	9.65	±1%
D-160 or 2048 (Write)	1414-1	217.6	24.0	16.0	±1%
D-160 or 2048 (Write)	1414-7	217.7	24.08	16.05	±1%
D-160 or 2048 (Read)	1414-1	204.8	24.0	16.0	±1%
D-160 or 2048 (Read)	1414-7	204.85	24.08	16.05	±1%
D-180 or 64 (Write)	1414-1	224.0	27.0	18.0	±1%
D-180 or 64 (Write)	1414-7	224.1	27.08	18.05	±1%
D-180 or 64 (Read)	1414-1	211.2	27.0	18.0	±1%
D-180 or 64 (Read)	1414-7	211.25	27.08	18.05	±1%
FSD-44	1414-1	4.4	-----	-----	±2%
FSD-44	1414-7	4.45	-----	-----	±2%
FSD-98	1414-1	9.8	-----	-----	±1%
FSD-98	1414-7	9.85	-----	-----	±1%

*1414-7 only

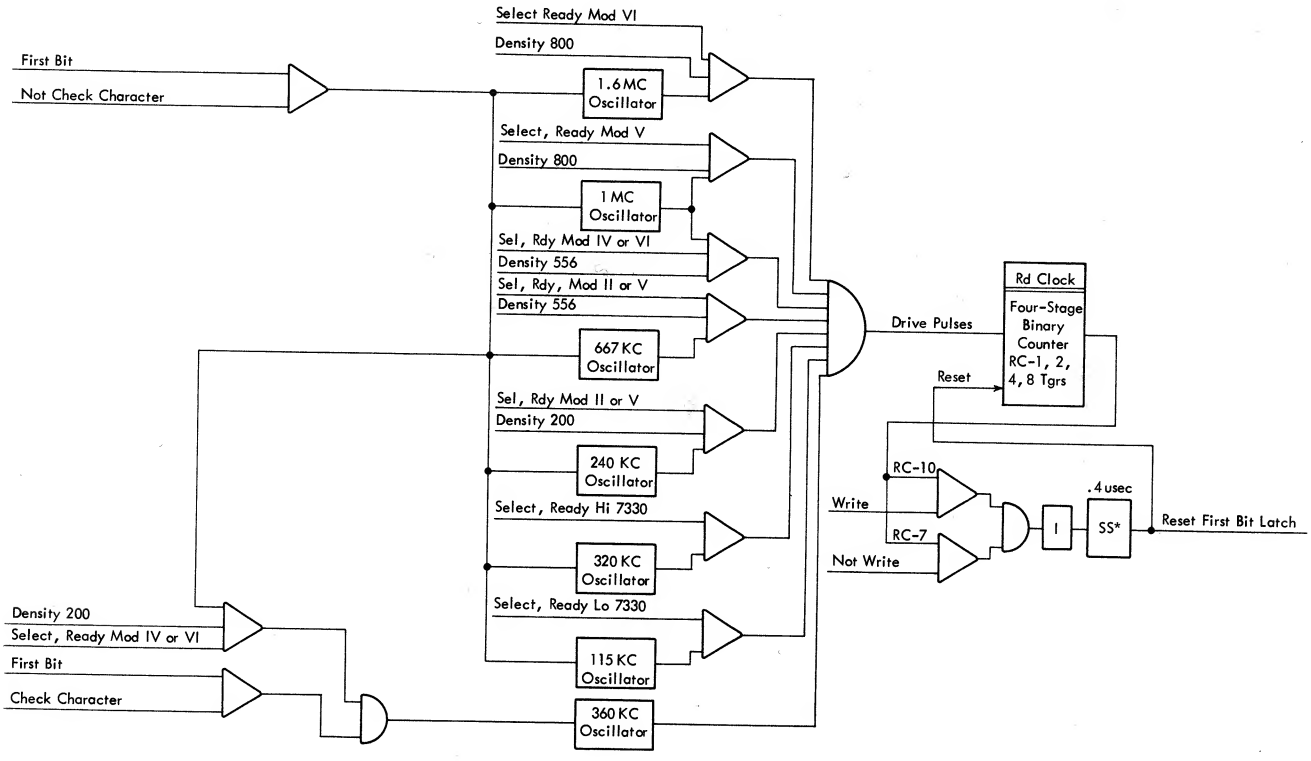
**Tolerance on all other delay counter microsecond timings except RDD-36 is ±1%; RDD-36 tolerance is ±2%

Figure 39. Delay Counter — Millisecond Outputs



*Singleshot fires when the RC-10 pulse (Write) or RC-7 pulse (Not Write) falls
**1414-1 with intermix and 800 cpi features

Figure 40 1414-1 Read Clock Drive



*Singleshot fires when the RC-10 pulse (Write) or RC-7 pulse (Not Write) falls
**1414-7 with intermix feature

Figure 41. 1414-7 Read Clock Drive

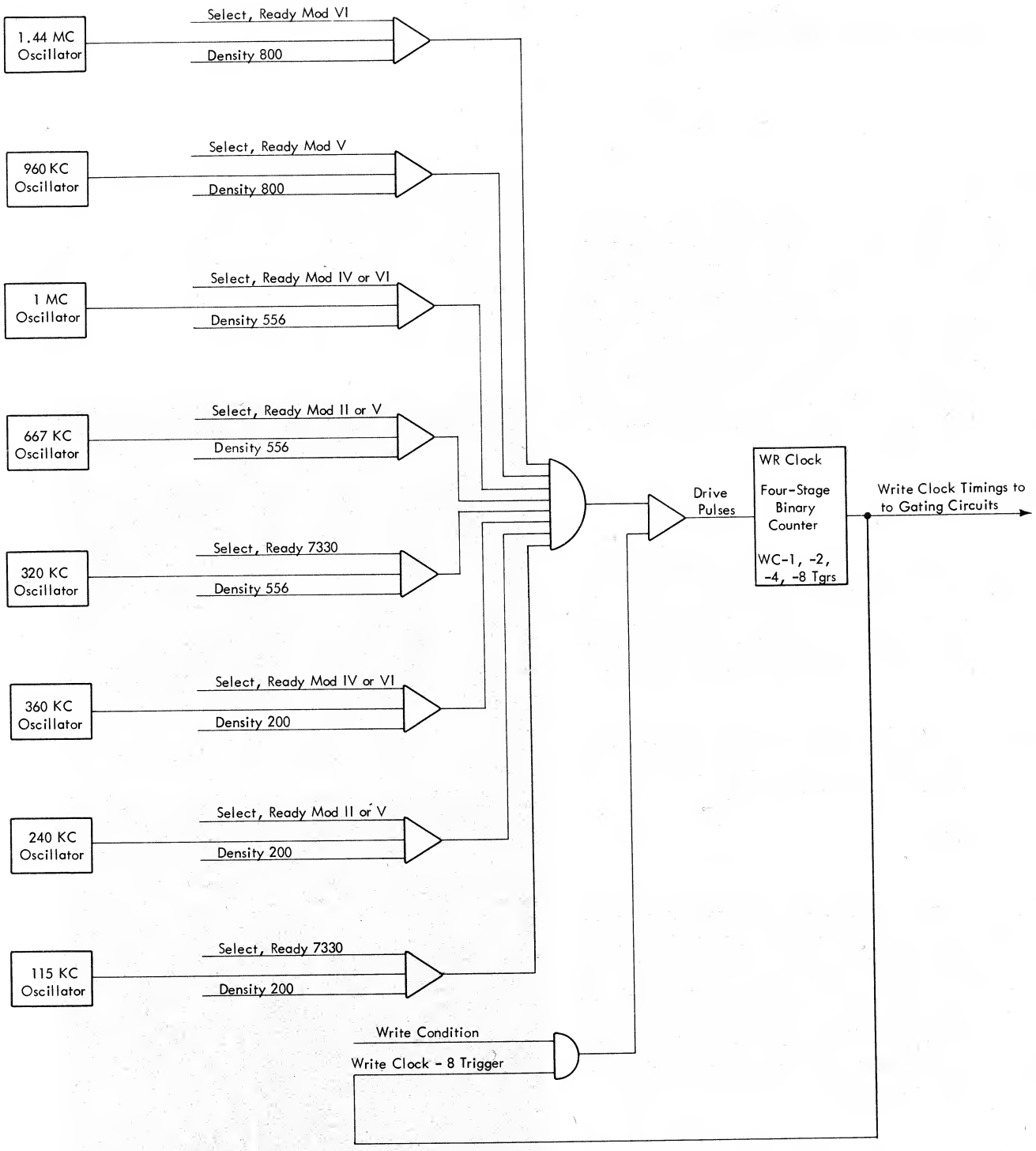


Figure 42. 1414-1 or 7 Write Clock Drive

CE Panel

In off-line operation, the customer engineer can duplicate all CPU commands to the tape synchronizer by operating CE panel controls. The CE panel (Figures 43 and 44) aids in checking tape synchronizer operation, making synchronizer adjustments, and locating failures. Indicators on the CE panel provide a visual indication of the status of control circuits in the tape synchronizer and in the CE control unit. Lights represent the state of each register, counter, clock, ring, and several control latches.

CE Panel Keys

START

When CE switches are set to select the desired operation, the START key must be pressed to initiate the operation. If the SINGLE CYCLE switch is off, the designated operation cycles repetitively, and the START key need not be pressed again during the operation.

RESET

The RESET key resets the CE control and conditions the TAU reset line (30.31.1). The START key must be pressed to begin the next CE operation.

CE Panel Switches

CE OP

The CE OP switch conditions the tape synchronizer for off-line operation, causing the synchronizer to accept commands from the CE panel. Only the STOP ON ERROR switch is active when the CE OP switch is off (68.05.1). The tape off-line indicators on the IBM 1415-1 and 2 Consoles (1410 and 7010 Systems) light when the CE OP switch is on; the tape synchronizer will not execute CPU commands.

SINGLE CYCLE

When the SINGLE CYCLE switch is off, the selected CE operation cycles repetitively. When the single cycle switch is on, the tape synchronizer performs one cycle of the designated operation and stops; the START key must be pressed again to begin the next cycle.

STOP ON ERROR

The STOP ON ERROR switch is operative in both on-line and off-line tape operations. When the switch is on, the manual stop on error line is conditioned to check the states of the error latch and the read-write register VRC latch. If the error latch is set:

1. The write RC-10 or read RC-7 reset line is held inactive until the system or the CE panel resets the tape operation to prevent resetting the A and B read registers.
2. Input paths to the read registers are blocked.

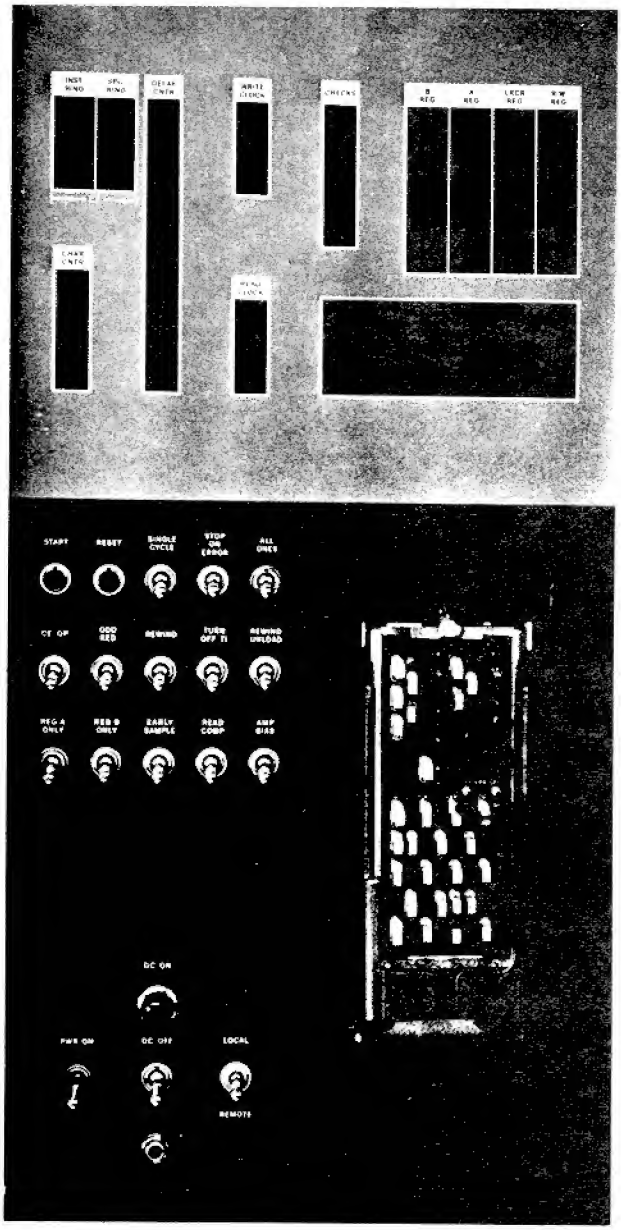


Figure 43. Tape Synchronizer CE Panel

3. The tape synchronizer busy line is held active.

4. An earlier read clock pulse samples the read register compare circuits.

5. If the read-write register VRC latch is set, the freeze read-write register line is conditioned, causing:

   a. The read condition only line to drop.

   b. The set and reset paths to the read-write register to be blocked.

At the end of the tape operation, the read-write registers contain the character or condition that caused the error.

When the STOP ON ERROR switch is on, the tape off line indicator on the 1415-1 and 2 consoles (1410 and 7010) light regardless of the position of the CE OP switch.

WRITE ALL ONES

The WRITE ALL ONES switch conditions the write data lines to the tape unit, causing the tape unit to write a seven bit character during each write cycle.

ODD REDUNDANCY

The ODD REDUNDANCY switch conditions the odd redundancy call line to turn on the odd redundancy latch in the tape synchronizer (40. 61. 1). The odd redundancy latch conditions all tape synchronizer VRC circuits to check for odd parity characters. When the latch is off, VRC circuits test for even parity characters.

REWIND

When the REWIND switch is on, "rewind call" is conditioned (60. 02. 1) to set the rewind latch. The tape synchronizer initiates a normal rewind operation on the selected tape unit.

TURN OFF TAPE INDICATOR (TI)

The TURN OFF TI switch generates the request signal (60. 50. 1) to turn off the tape indicator on the selected tape unit.

REWIND UNLOAD

When the REWIND UNLOAD switch is on, "rewind unload call" is conditioned (60. 02. 1) to turn on the rewind unload latch. The tape synchronizer initiates a normal rewind operation; 729 tape units unload tape when load point is sensed.

REGISTER A ONLY

Normally, in read only operations, the character in read register B transfers to the LRCR and read-write register when the character in read register contains a VRC error. The REGISTER A ONLY switch generates the register A only line to block the output of the read register A VRC circuit and allow read register A to set

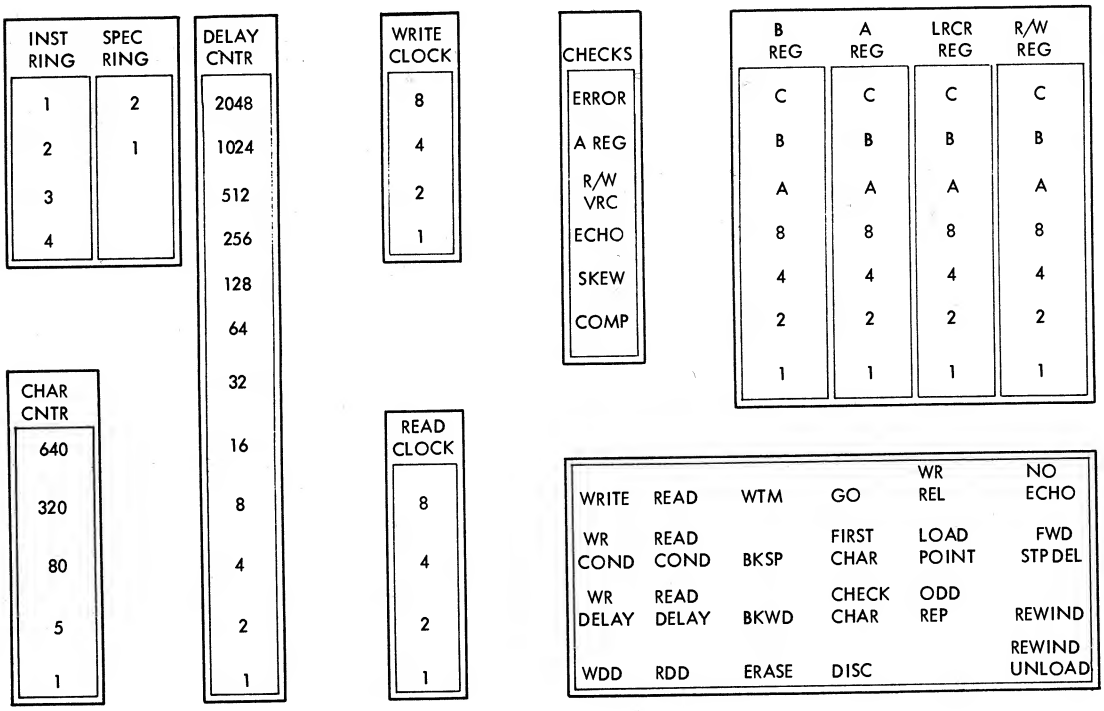


Figure 44. Tape Synchronizer CE Panel Indicators

the LRCR and, in read only operations, the read-write register each character cycle, regardless of the vertical structure of the character in the A register.

REGISTER B ONLY

By forcing an A register VRC indication each character cycle, the REG B ONLY switch causes the character in read register B to transfer to the LRCR and, in read only operations, the read-write register. The REG B ONLY switch should not be used in a write operation when the STOP ON ERROR switch is on. In a read only operation, B register random pickup can occur due to the low-clip level of the B register. See AMP BIAS switch operation.

EARLY SAMPLE

The EARLY SAMPLE switch causes the skew gate latch in the tape synchronizer (10. 31. 1) to turn on during a read only operation. The EARLY SAMPLE switch also allows an A register VRC indication to turn on the tape synchronizer error latch in a read only operation.

READ COMPARE

In a write operation, the character in read register A is compared to the character in read register B during each character cycle. If the characters are not identical, the check latch is set, indicating a compare error (50. 30. 1). The READ COMP switch causes the tape synchronizer to make the read register compare check during a read only operation.

The READ COMP switch should be used with discretion. Because the low-clip level for read register B register is only 7.5%, a signal or noise in the amplifier track above 0.6 volts peak-to-peak is set into the B register. Therefore, B register random pickup might occur during read compare operations. This is especially true for higher tape drives preamplifier settings for 800 cpi. See AMP BIAS switch operation.

AMP BIAS

The AMP BIAS switch alters input acceptance levels for tape synchronizer final amplifiers. In a read operation, final amplifiers are conditioned to accept data at normal write operation levels. In a write operation, final amplifiers are conditioned to accept data at normal read operation levels.

The AMP BIAS switch should be used only during read operations. When this switch is used in conjunction with the READ COMP or REG B ONLY switch, it prevents B register pickup, but the probability of A register (high-clip level) random dropout is greatly increased. New clip levels that EC-112238 establish greatly improve the dropout condition, but occasional dropouts may still occur.

CE Control Plug Board

The CE Control Plug Board (Figure 45) permits customer engineers to manually program tape synchronizer operations. A control panel program can select a tape unit, designate CE tape operations, vary the length of tape records, and select bit configurations for each of five characters. Two rings and a counter in the CE control circuits condition the control panel hubs. Each ring and the counter operate separately.

Instruction Ring

The CE reset line resets the four-stage instruction ring counter; the busy line dropping advances the counter (Figure 46). The CE reset line turns on the first stage of the counter and turns off the other three stages. Instruction ring-1 select-out and instruction ring-1 instruction out control plug board hubs are conditioned immediately after the counter is reset. When the START key is pressed, the control line begins the designated operation. The tape synchronizer conditions the busy line and holds "busy" active to the end of the operation. The busy line dropping advances the instruction counter in loops (1, 2, 3, 4, 1, 2, 3, 4, 1, 2, 3, 4, etc.) until: the RESET button is pressed; the special ring is conditioned; or the SINGLE CYCLE switch is turned on. All four ring positions must be used for continuous run operation.

SELECT-OUT AND SELECT-IN HUBS

The instruction ring or the special ring conditions the select-out hubs. Select-out hubs must be wired to select-in hubs to designate a tape unit to perform the CE operation. The ten select-in hubs numbers correspond to the ten tape units that the tape synchronizer controls.

INSTRUCTION-OUT AND INSTRUCTION-IN HUBS

The instruction ring or the special ring conditions the instruction-out hubs. Instruction-out hubs must be wired to instruction-in hubs to select the desired CE tape operation. When the START pushbutton is pressed, the "CE pulse" combines with the output of an instruction-in hub to send appropriate control lines to the tape synchronizer.

NOTE: when instruction-out hub 1 is wired to erase, the fall of "busy" from the "erase call" causes the instruction ring to step after reset.

Special Ring

The special ring is a two-stage counter used for special CE programming when an error is detected. The plug board error hub must be connected to the special-routine hub to condition the special ring. When the tape synchronizer error latch (50. 50. 1) is set, the special ring causes the tape synchronizer to perform

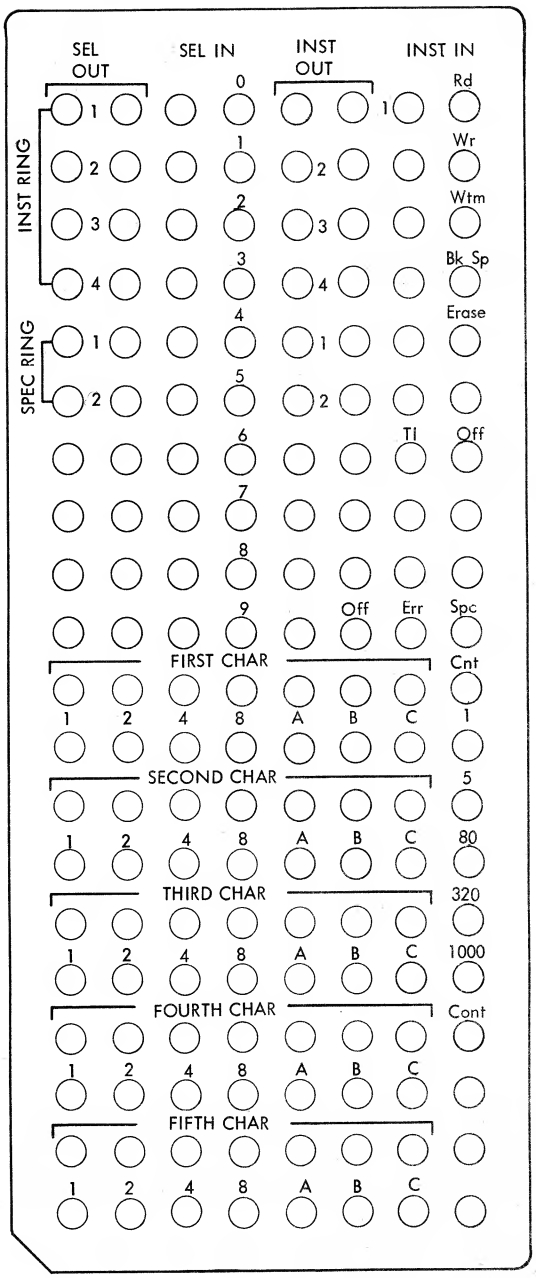


Figure 45. CE Control Plug Board

alternate operations designated on the plug board. For example, the CE plug board might specify backspace and read, backspace and write, or backspace and erase when the tape synchronizer detects an error in the main operation. The special routine hub should be connected to the off hub when the special ring is not used.

Character Counter

The thirteen-stage character counter controls the variable length record and the sequence of the five plug board characters.

COUNT HUBS

Count hubs control the timing of the disconnect call signal to the tape synchronizer (68. 32. 1) to end the operation. The count (CNT) hub must be wired from one of the count number hubs (1, 5, 80, 320, 1000, or CONT). Count number hubs, conditioned by the character counter, select the length of the records. If the STOP ON ERROR switch is on, an error conditions "disconnect call" in continuous write operation.

CHARACTER HUBS

Five sets of character hubs are available. Any bit configuration can be wired for each of the five characters. If the CE program requires more than five characters, outputs from the character hubs are repeated (1, 2, 3, 4, 5, 1, 2, 3, 4, 5, etc.).

TI OFF

The TI OFF hub is used to check the end of tape photocell in the tape unit. When the tape indicator (TI) light turns on, the TI OFF hub may be wired. When the TI OFF hub is wired, a plugged program of a double backspace, read, then write causes the tape unit to cycle to the end of file; the photocell turns on and off.

1414-1 (Without 800 CPI Feature) and 2 Clipping Level Checks

Tape synchronizer clipping level checks provide tests for clipper cards and clipping acceptance levels; the checks do not test the entire track. Clipping level checks are valid only for the clipping levels established with EC-112238. Because AC signals cause erroneous readings, bits should not enter the track during the read check of a write operation or a read only operation.

Write Clipping Level Check

1. Rotate the tape unit selector to 0; rewind the tape unit to load point.
2. Set the CE OP switch up; set all other functional switches down.
3. Wire jumpers on the CE control plug board as follows:

SEL OUT 1 to SEL OUT 2
SEL OUT 2 to SEL OUT 3
SEL OUT 3 to SEL OUT 4
SEL OUT 1 to SEL IN 0
INST OUT 1 to INST OUT 2
INST OUT 2 to INST OUT 3
INST OUT 3 to INST OUT 4
INST OUT 1 to INST IN WRITE
SPC to OFF
NO CHAR BITS plugged
CNT to CONT

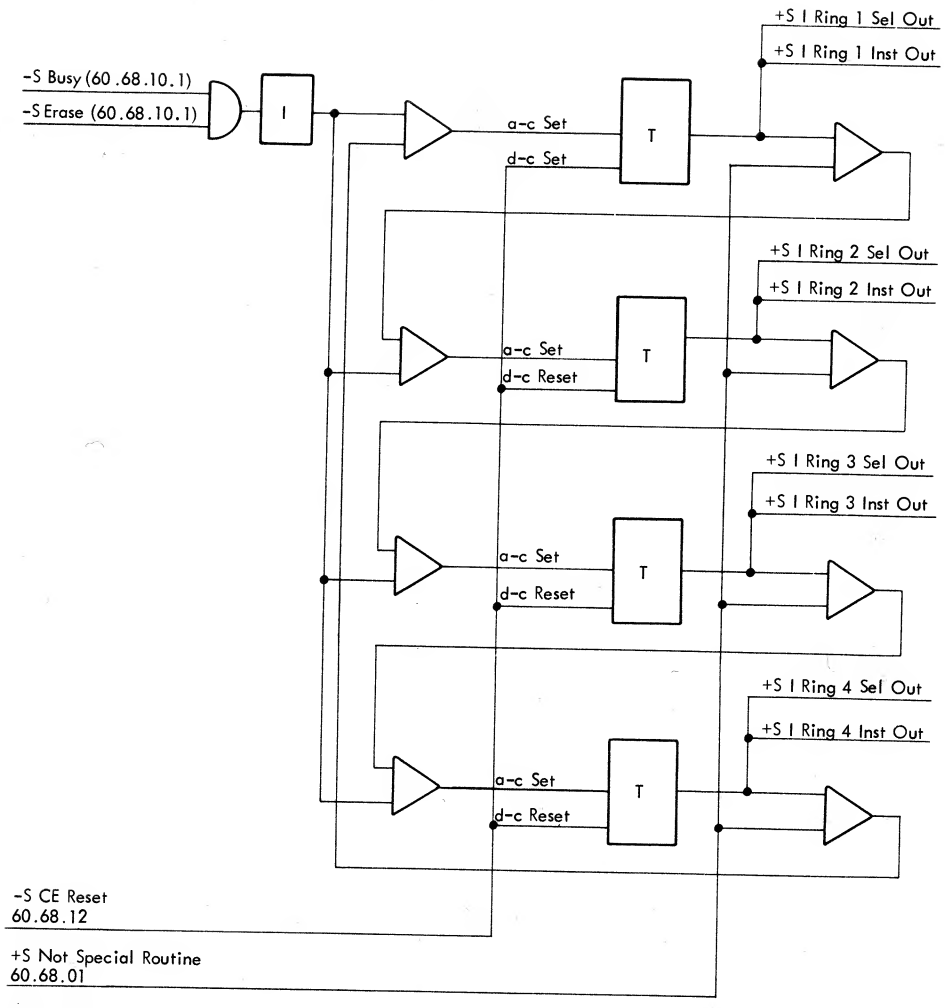


Figure 46. Instruction Ring

4. Press 1414 RESET key; observe that the CE control panel LOAD POINT indicator is on.

5. Press 1414 START key; observe that the ECHO ERROR indicator is on.

6. Adjust a 20K ohms/volt multimeter for minimum voltage scale above 2.5 volts. Connect meter leads to pins listed in Figure 47, and observe meter for indicated outputs.

NOTE: If meter readings do not conform to values listed in Figure 47, perform Clipping Level Error Check.

Read Clipping Level Check

1. Perform the first steps listed under Write Clipping Level Check.

2. Press the 1414 RESET key; set the REWIND switch up, then down.

3. Remove jumper connecting INST OUT 1 to INST IN WRITE on control plug boards.

4. Insert jumper from INST OUT 1 to INST IN READ.

5. Wait for LOAD POINT indicator on CE control panel to light, then press the 1414 START key. Check to see that no bits are in the read-write register and that the read clock is not running.

6. Adjust the multimeter for minimum voltage scale above 2.0 volts. Connect meter leads to pins listed in Figure 48 and observe meter for indicated outputs.

7. If the last few readings are high, check to see that the read clock and read-write register indicators are off. If the indicators are lighted, press the RESET key; set the REWIND switch up and down; repeat steps 10 and 11.

NOTE: If meter readings do not conform to values listed in Figure 48, perform Clipping Level Error Check.

Clipping Level Error Check

Perform the appropriate steps in accordance with the error condition encountered in the clipping level read or write check.

Meter Lead Connections (Panel 6)		Acceptance Range Positive Voltage Referenced to -12v
Negative	Positive	
E05M	E05C	2.06 to 2.50
E05M	E05F	1.33 to 1.78
E07M	E07C	2.06 to 2.50
E07M	E07F	1.33 to 1.78
E09M	E09C	2.06 to 2.50
E09M	E09F	1.33 to 1.78
E12M	E12C	2.06 to 2.50
E12M	E12F	1.33 to 1.78
E14M	E14C	2.06 to 2.50
E14M	E14F	1.33 to 1.78
E16M	E16C	2.06 to 2.50
E16M	E16F	1.33 to 1.78
E18M	E18C	2.06 to 2.50
E18M	E18F	1.33 to 1.78

*without 800 cpi feature

Figure 47. Write Clipping Level Check for 1414-1 and 2

Meter Lead Connections (Panel 6)		Acceptance Range Positive Voltage Referenced to -12v
Negative	Positive	
E05M	E05C	1.69 to 2.00
E05M	E05F*	0.00 to 0.14
E07M	E07C	1.69 to 2.00
E07M	E07F*	0.00 to 0.14
E09M	E09C	1.69 to 2.00
E09M	E09F*	0.00 to 0.14
E12M	E12C	1.69 to 2.00
E12M	E12F*	0.00 to 0.14
E14M	E14C	1.69 to 2.00
E14M	E14F*	0.00 to 0.14
E16M	E16C	1.69 to 2.00
E16M	E16F*	0.00 to 0.14
E18M	E18C	1.69 to 2.00
E18M	E18F*	0.00 to 0.14

*if necessary, adjust multimeter to minimum scale for accurate reading.
**without 800 cpi feature

Figure 48. Read Clipping Level Check for 1414-1 and 2

If readings for both read and write are the same, and either the read or write voltages are correct:

1. Scope chassis C5BF (input pin F acceptance card YCA 60. 40. 10. 1); level should be ground potential for write and negative for read.
2. Press 1414 RESET key.
3. Change INST OUT status.
4. Press 1414 START key. If input levels are correct, YCA card (60. 40. 10. 1) is probably defective. If input levels are incorrect, observe WRITE indicator on CE panel to see that indicator is on during write and off during read. If WRITE indicator remains on during read, or fails to light during write, check the write latch (60. 60. 30. 1). If the write latch is functioning properly, the DHH card (location 5A, 5B, and 4A, logic page 60. 40. 10. 1) is probably at fault.

If voltages for both read and write are the same and neither is correct, or all readings are off by the same amount, check acceptance card YCA (40. 10. 1).

If one voltage reading is high or low on either read or write or both, check clipper card YJC (40. 10. 1).

If the read and write voltages are reversed, check the AMP BIAS switch on the CE panel.

Tape Synchronizer Error Circuits Check

To test the operation of error circuits in the tape synchronizer:

1. Turn on power switches on the CE panel.
2. Turn on CE OP switch.
3. Turn on SINGLE CYCLE switch. STOP ON ERROR switch must be OFF.
4. Wire the control plug board to select a tape drive to write no bits (no plugs in CE control bit hubs) and to write a fixed record length.
5. Turn on ODD RED switch.
6. Condition the selected tape unit for ready status; use a CE work tape.
7. Remove the high-clip amplifier card from any track to cause an A reg VRC error.
8. Press the START pushbutton to begin the operation and reset the A reg VRC error.
9. Observe the CE indicator panel to see that the following conditions are registered.
   - R-W VRC error
   - LRCR error
   - Echo error
   - Compare error
   - Skew error
10. Press the RESET key.
11. Repeat steps 7 through 10, removing a different high-clip amplifier card each time until the procedure has been performed once for each tape track.

Appendix

1414 Tape Synchronizer (Models 1 and 2) Second Level Diagrams

FIGURE	TITLE
180	Reference Sheet
181	Write Controls 1
182	Write Controls 2
183	Read Controls 1
184	Read Controls 2
185	Backspace, Erase, Rewind, Rewind Unload
186	Write Clock and Delay Counter Oscillator Gating
187	Delay Counter
188	Read Disconnect Delay, Forward Stop Delay, and Check Character
189	Go and Tape Drive Input-Output Lines
190	Final Amplifiers, A and B Read Registers, R-W Reg, and LRCR Reg
191	Error Circuits 1
192	Error Circuits 2
T80	Tape Unit Response Logic

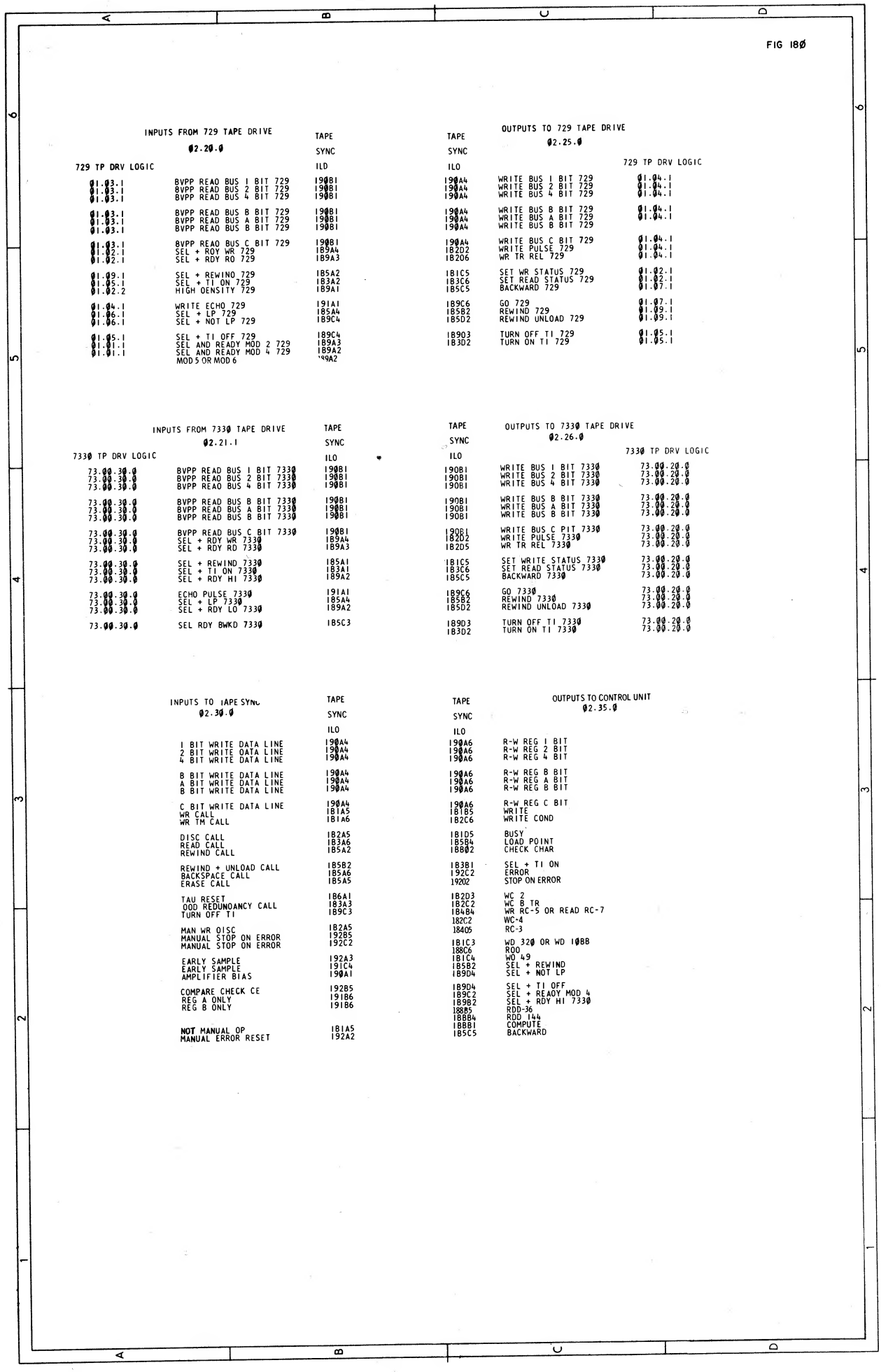


FIG 180

INPUTS FROM 729 TAPE DRIVE
02.20.0

729 TP DRV LOGIC		TAPE SYNC ILD
01.03.1	BVPP READ BUS 1 BIT 729	190B1
01.03.1	BVPP READ BUS 2 BIT 729	190B1
01.03.1	BVPP READ BUS 4 BIT 729	190B1
01.03.1	BVPP READ BUS B BIT 729	190B1
01.03.1	BVPP READ BUS A BIT 729	190B1
01.03.1	BVPP READ BUS B BIT 729	190B1
01.03.1	BVPP READ BUS C BIT 729	190B1
01.02.1	SEL + RDY WR 729	189A4
01.02.1	SEL + RDY RD 729	189A3
01.09.1	SEL + REWIND 729	185A2
01.05.1	SEL + TI ON 729	183A2
01.02.2	HIGH DENSITY 729	189A1
01.04.1	WRITE ECHO 729	191A1
01.06.1	SEL + LP 729	185A4
01.06.1	SEL + NOT LP 729	189C4
01.05.1	SEL + TI OFF 729	189C4
01.01.1	SEL AND READY MOD 2 729	189A3
01.01.1	SEL AND READY MOD 4 729	189A2
	MOD 5 OR MOD 6	199A2

OUTPUTS TO 729 TAPE DRIVE
02.25.0

TAPE SYNC ILO		729 TP DRV LOGIC
190A4	WRITE BUS 1 BIT 729	01.04.1
190A4	WRITE BUS 2 BIT 729	01.04.1
190A4	WRITE BUS 4 BIT 729	01.04.1
190A4	WRITE BUS B BIT 729	01.04.1
190A4	WRITE BUS A BIT 729	01.04.1
190A4	WRITE BUS B BIT 729	
190A4	WRITE BUS C BIT 729	01.04.1
182D2	WRITE PULSE 729	01.04.1
182D6	WR TR REL 729	01.04.1
181C5	SET WR STATUS 729	01.02.1
183C6	SET READ STATUS 729	01.02.1
185C5	BACKWARD 729	01.07.1
189C6	GO 729	01.07.1
185B2	REWIND 729	01.09.1
185D2	REWIND UNLOAD 729	01.09.1
189D3	TURN OFF TI 729	01.05.1
183D2	TURN ON TI 729	01.05.1

INPUTS FROM 7330 TAPE DRIVE
02.21.1

7330 TP DRV LOGIC		TAPE SYNC ILO
73.00.30.0	BVPP READ BUS 1 BIT 7330	190B1
73.00.30.0	BVPP READ BUS 2 BIT 7330	190B1
73.00.30.0	BVPP READ BUS 4 BIT 7330	190B1
73.00.30.0	BVPP READ BUS B BIT 7330	190B1
73.00.30.0	BVPP READ BUS A BIT 7330	190B1
73.00.30.0	BVPP READ BUS B BIT 7330	190B1
73.00.30.0	BVPP READ BUS C BIT 7330	190B1
73.00.30.0	SEL + RDY WR 7330	189A4
73.00.30.0	SEL + RDY RD 7330	189A3
73.00.30.0	SEL + REWIND 7330	185A1
73.00.30.0	SEL + TI ON 7330	183A1
73.00.30.0	SEL + RDY HI 7330	189A2
73.00.30.0	ECHO PULSE 7330	191A1
73.00.30.0	SEL + LP 7330	185A4
73.00.30.0	SEL + RDY LO 7330	189A2
73.00.30.0	SEL RDY BWKD 7330	185C3

OUTPUTS TO 7330 TAPE DRIVE
02.26.0

TAPE SYNC ILO		7330 TP DRV LOGIC
190B1	WRITE BUS 1 BIT 7330	73.00.20.0
190B1	WRITE BUS 2 BIT 7330	73.00.20.0
190B1	WRITE BUS 4 BIT 7330	73.00.20.0
190B1	WRITE BUS B BIT 7330	73.00.20.0
190B1	WRITE BUS A BIT 7330	73.00.20.0
190B1	WRITE BUS B BIT 7330	73.00.20.0
190B1	WRITE BUS C PIT 7330	73.00.20.0
182D2	WRITE PULSE 7330	73.00.20.0
182D5	WR TR REL 7330	73.00.20.0
181C5	SET WRITE STATUS 7330	73.00.20.0
183C6	SET READ STATUS 7330	73.00.20.0
185C5	BACKWARD 7330	73.00.20.0
189C6	GO 7330	73.00.20.0
185B2	REWIND 7330	73.00.20.0
185D2	REWIND UNLOAD 7330	73.00.20.0
189D3	TURN OFF TI 7330	73.00.20.0
183D2	TURN ON TI 7330	73.00.20.0

INPUTS TO TAPE SYNC
02.30.0

	TAPE SYNC ILO
1 BIT WRITE DATA LINE	190A4
2 BIT WRITE DATA LINE	190A4
4 BIT WRITE DATA LINE	190A4
B BIT WRITE DATA LINE	190A4
A BIT WRITE DATA LINE	190A4
B BIT WRITE DATA LINE	190A4
C BIT WRITE DATA LINE	190A4
WR CALL	181A5
WR TM CALL	181A6
DISC CALL	182A5
READ CALL	183A6
REWIND CALL	185A2
REWIND + UNLOAD CALL	185B2
BACKSPACE CALL	185A6
ERASE CALL	185A5
TAU RESET	186A1
OOD REDUNDANCY CALL	183A3
TURN OFF TI	189C3
MAN WR OISC	182A5
MANUAL STOP ON ERROR	192B5
MANUAL STOP ON ERROR	192C2
EARLY SAMPLE	192A3
EARLY SAMPLE	191C4
AMPLIFIER BIAS	190A1
COMPARE CHECK CE	192B5
REG A ONLY	191B6
REG B ONLY	191B6
NOT MANUAL OP	181A5
MANUAL ERROR RESET	192A2

OUTPUTS TO CONTROL UNIT
02.35.0

TAPE SYNC ILO	
190A6	R-W REG 1 BIT
190A6	R-W REG 2 BIT
190A6	R-W REG 4 BIT
190A6	R-W REG B BIT
190A6	R-W REG A BIT
190A6	R-W REG B BIT
190A6	R-W REG C BIT
181B5	WRITE
182C6	WRITE COND
181D5	BUSY
185B4	LOAD POINT
188Ø2	CHECK CHAR
183B1	SEL + TI ON
192C2	ERROR
19202	STOP ON ERROR
182D3	WC 2
182C2	WC B TR
184B4	WR RC-5 OR READ RC-7
182C2	WC-4
18405	RC-3
181C3	WD 32Ø OR WD 1ØBB
188C6	ROO
181C4	WD 49
185B2	SEL + REWIND
189D4	SEL + NOT LP
189D4	SEL + TI OFF
189C2	SEL + REAOY MOD 4
189B2	SEL + RDY HI 7330
18885	RDD-36
188B4	RDD 144
18881	COMPUTE
185C5	BACKWARD

Figure 180. Reference

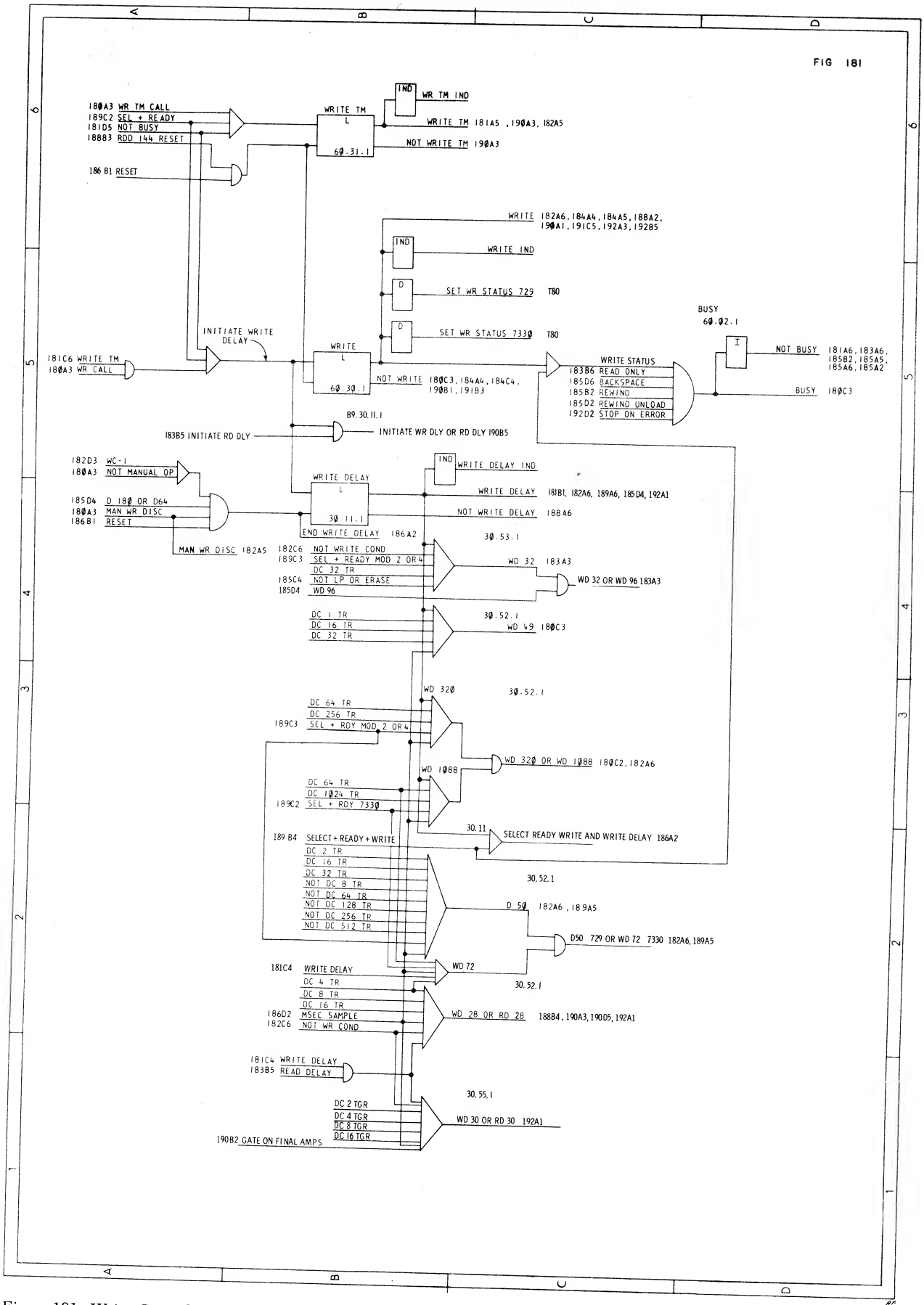


Figure 181. Write Controls I

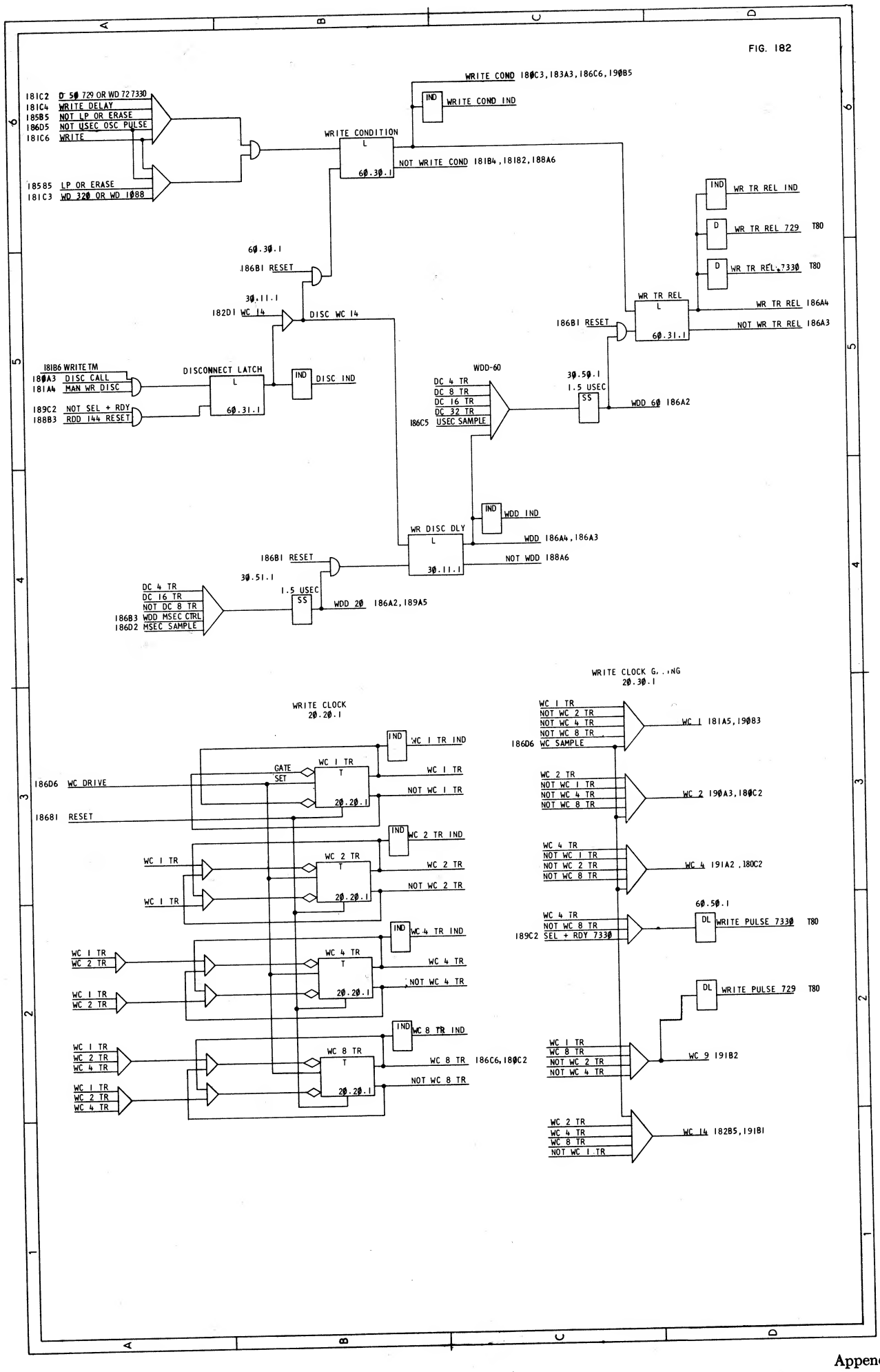


Figure 182. Write Controls II

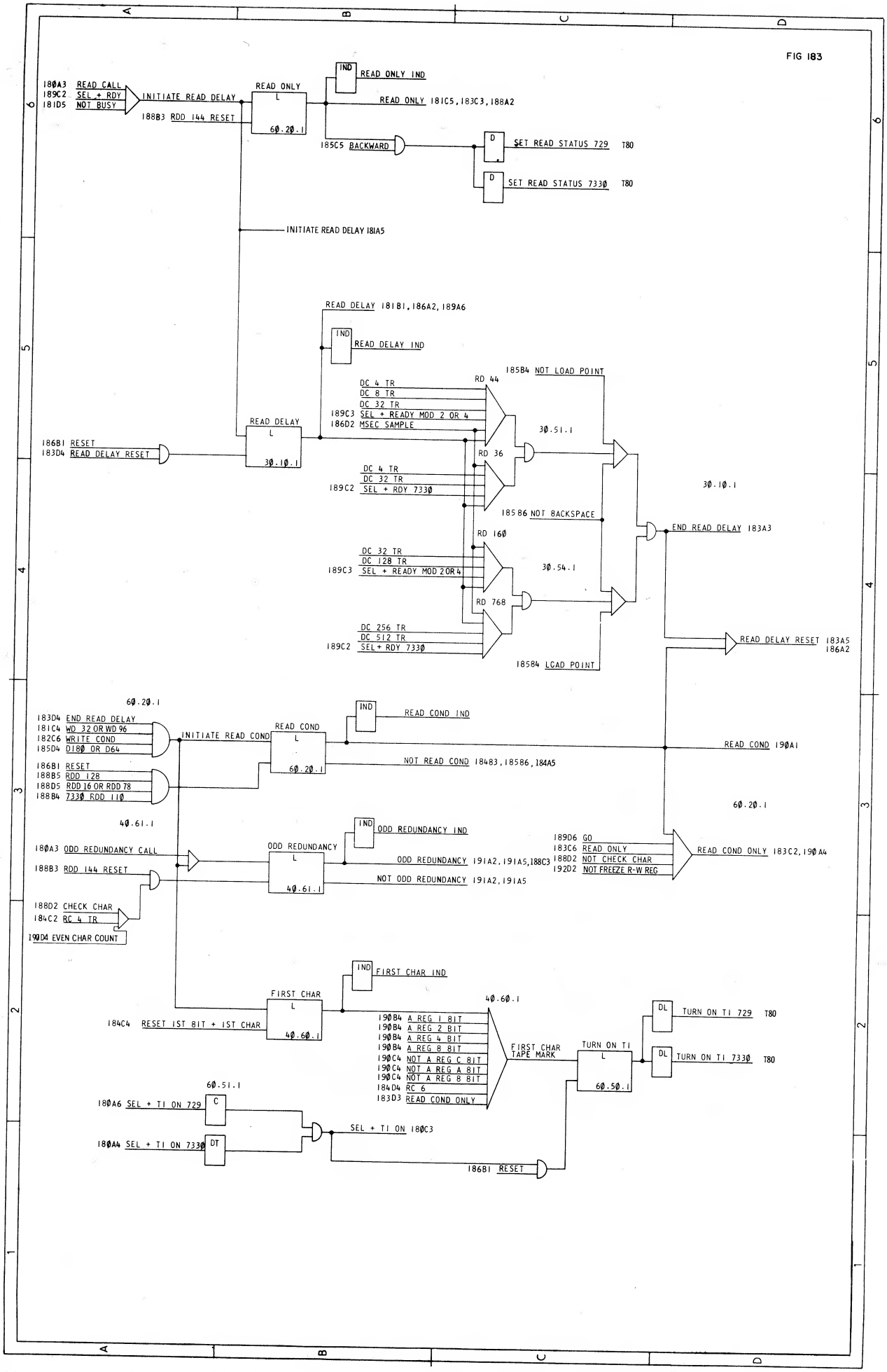


Figure 183. Read Controls I

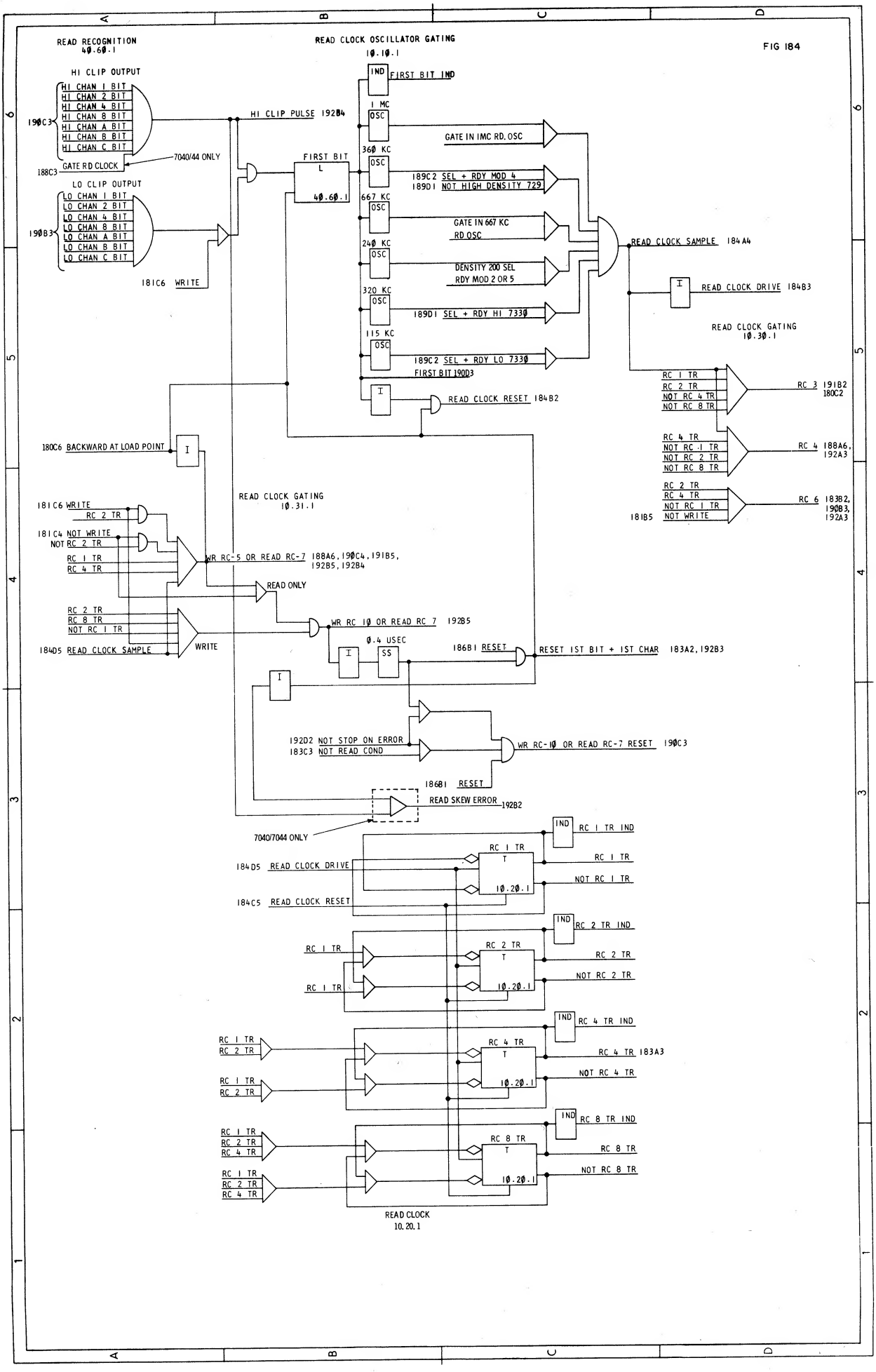
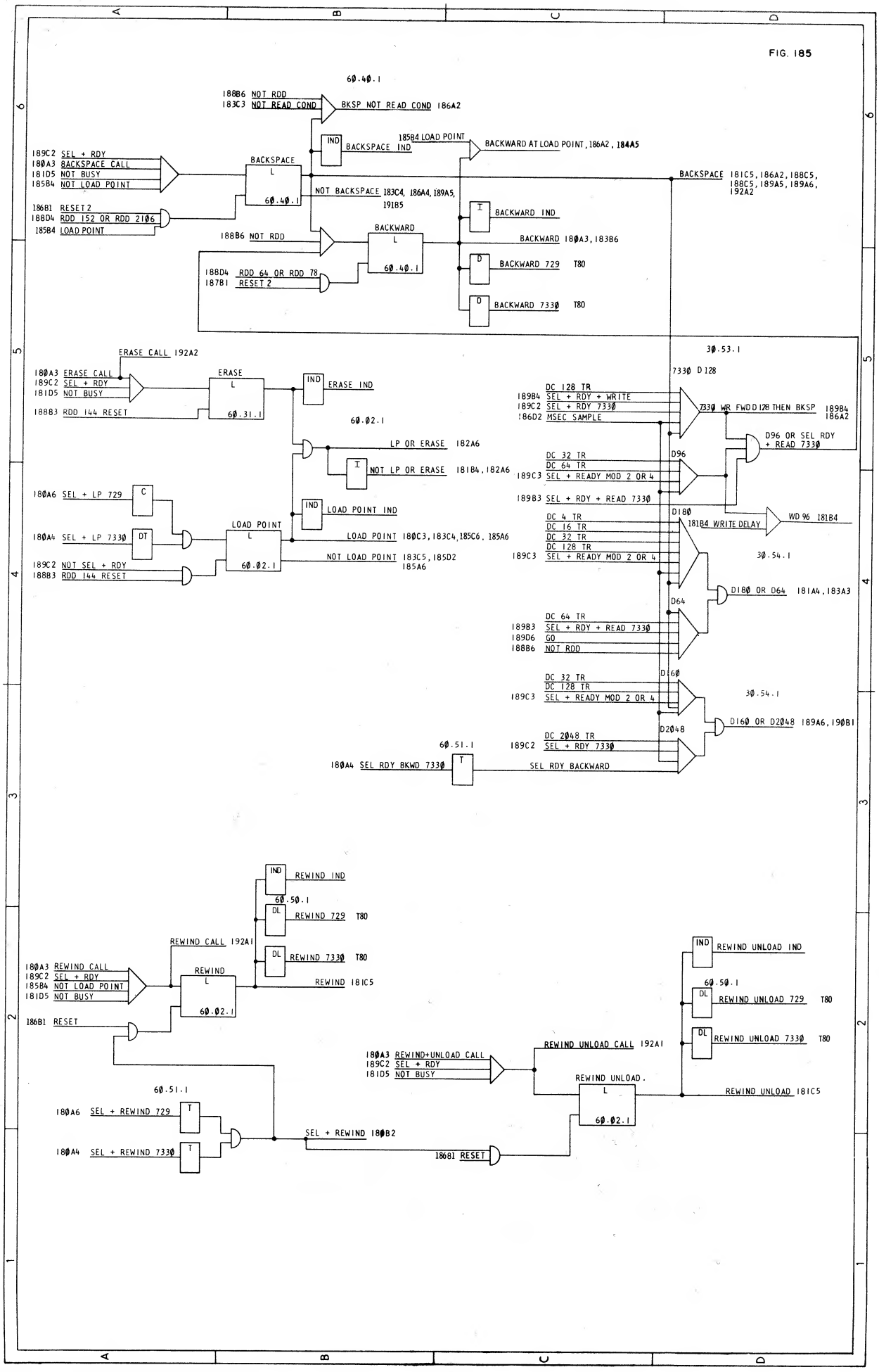


Figure 184. Read Controls II



100 Figure 185. Unit Control

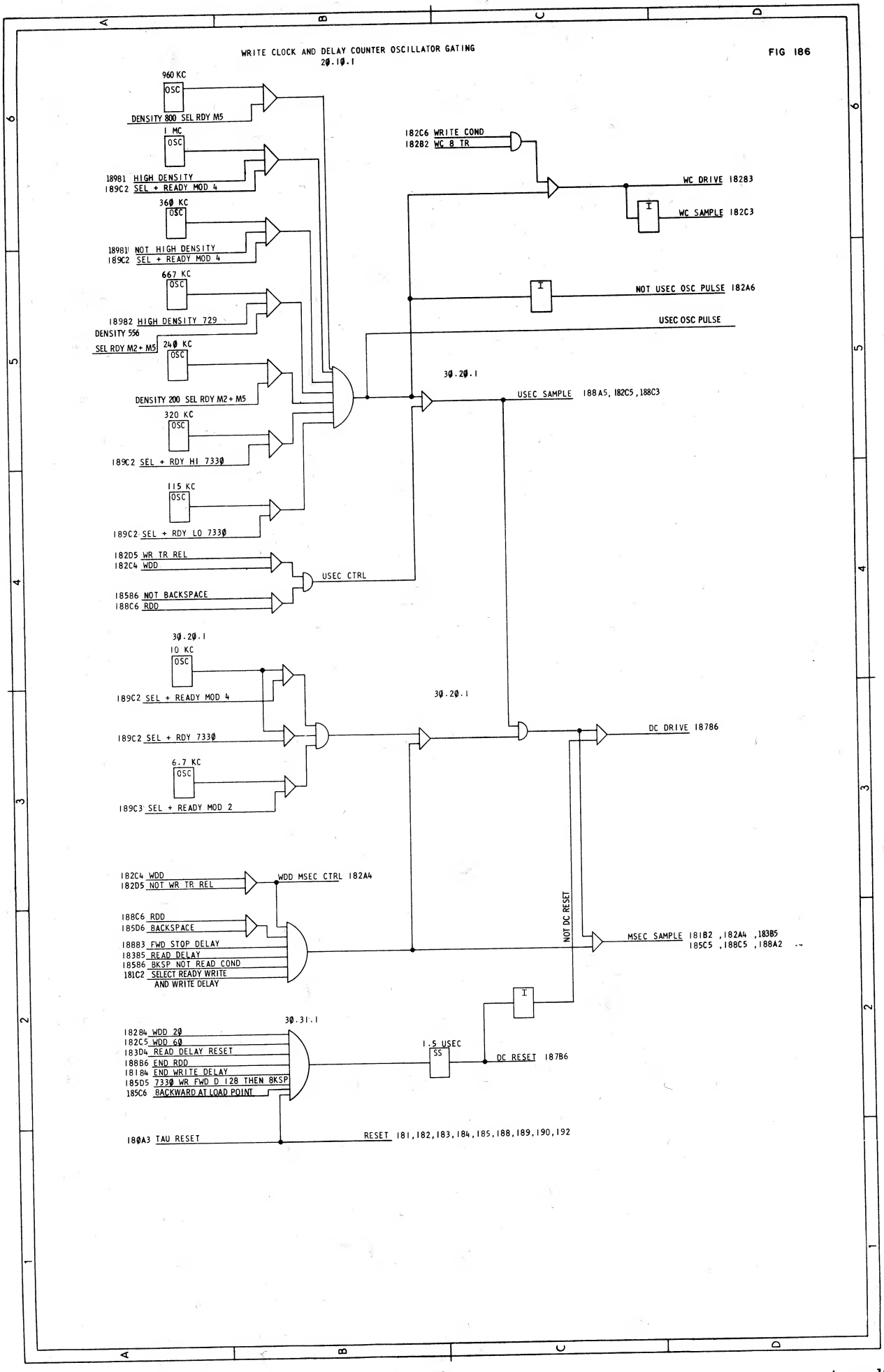


Figure 186. Write Clock and Delay Counter Oscillator Gating

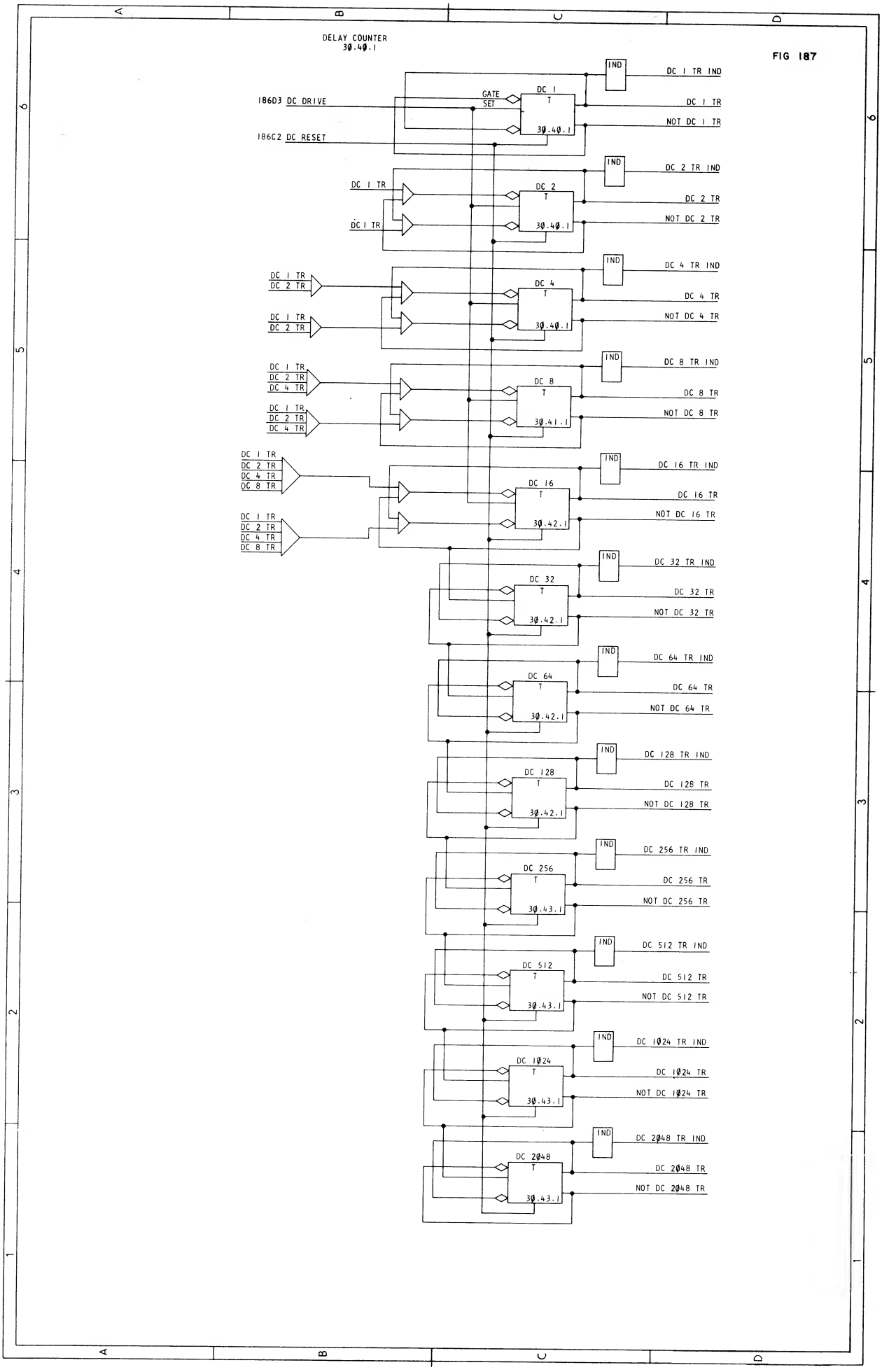


Figure 187. Delay Counter

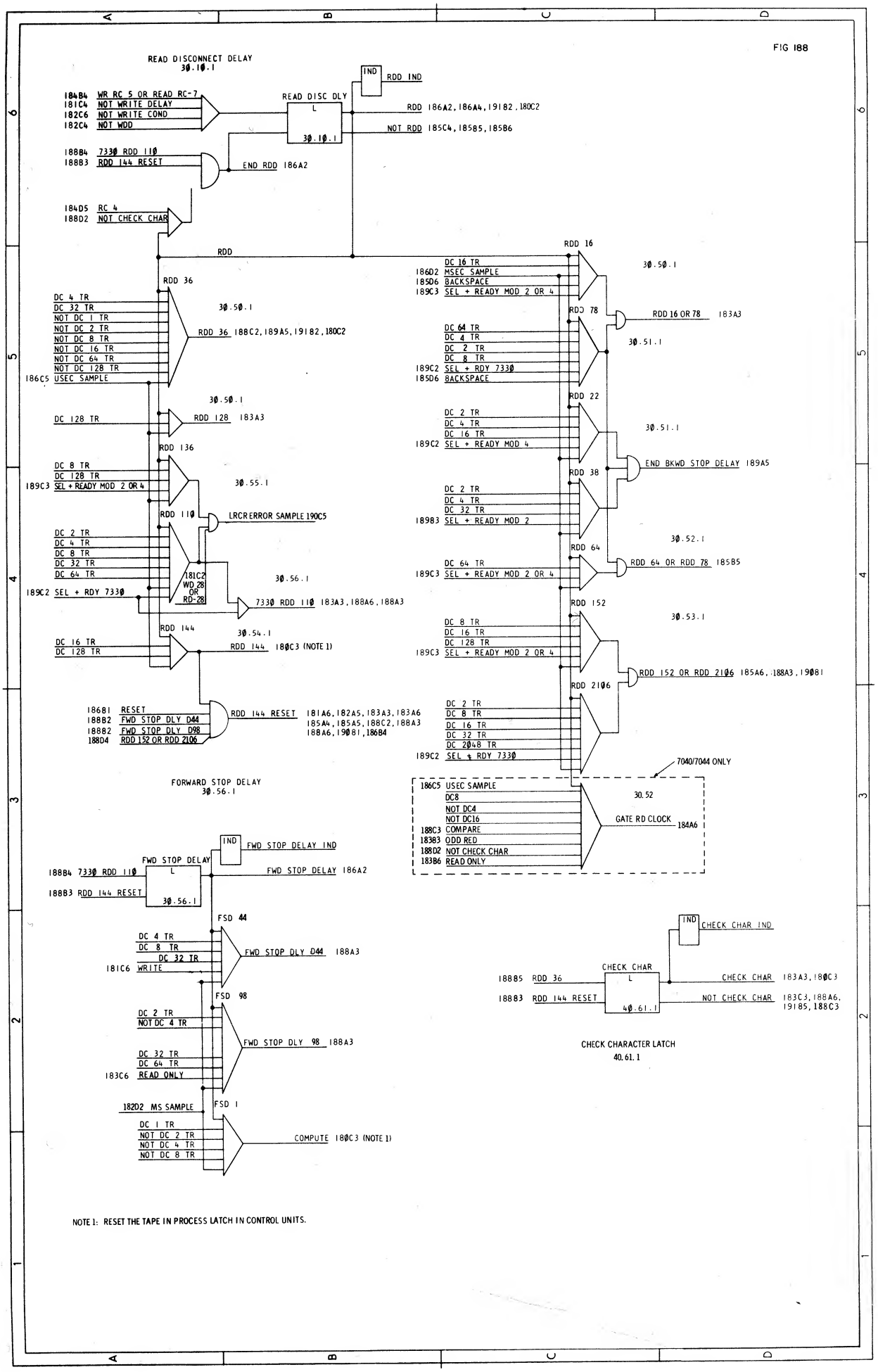


Figure 188. RDD, FSD, and Check Character

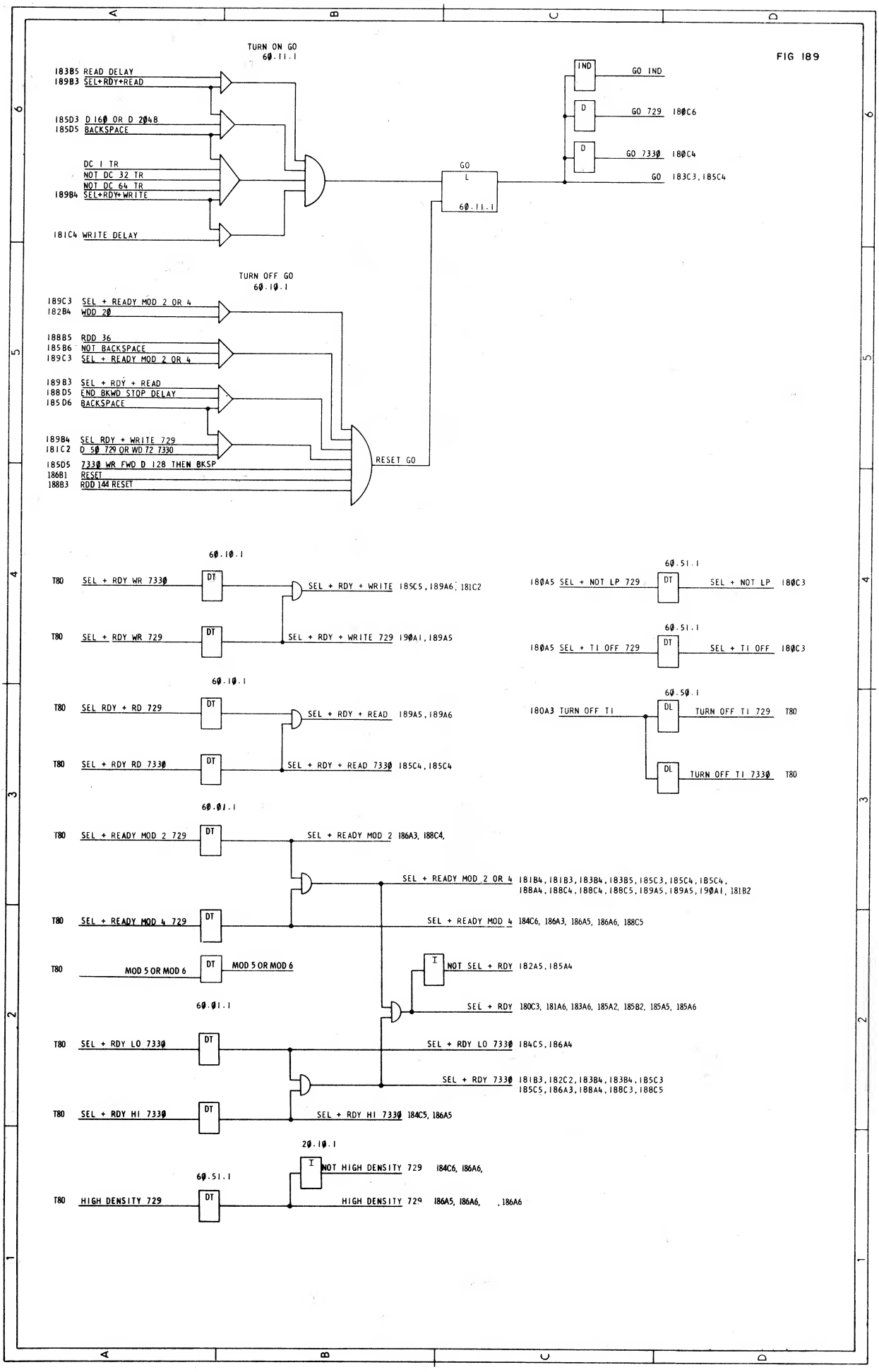


Figure 189. Go and Tape Drive Inputs

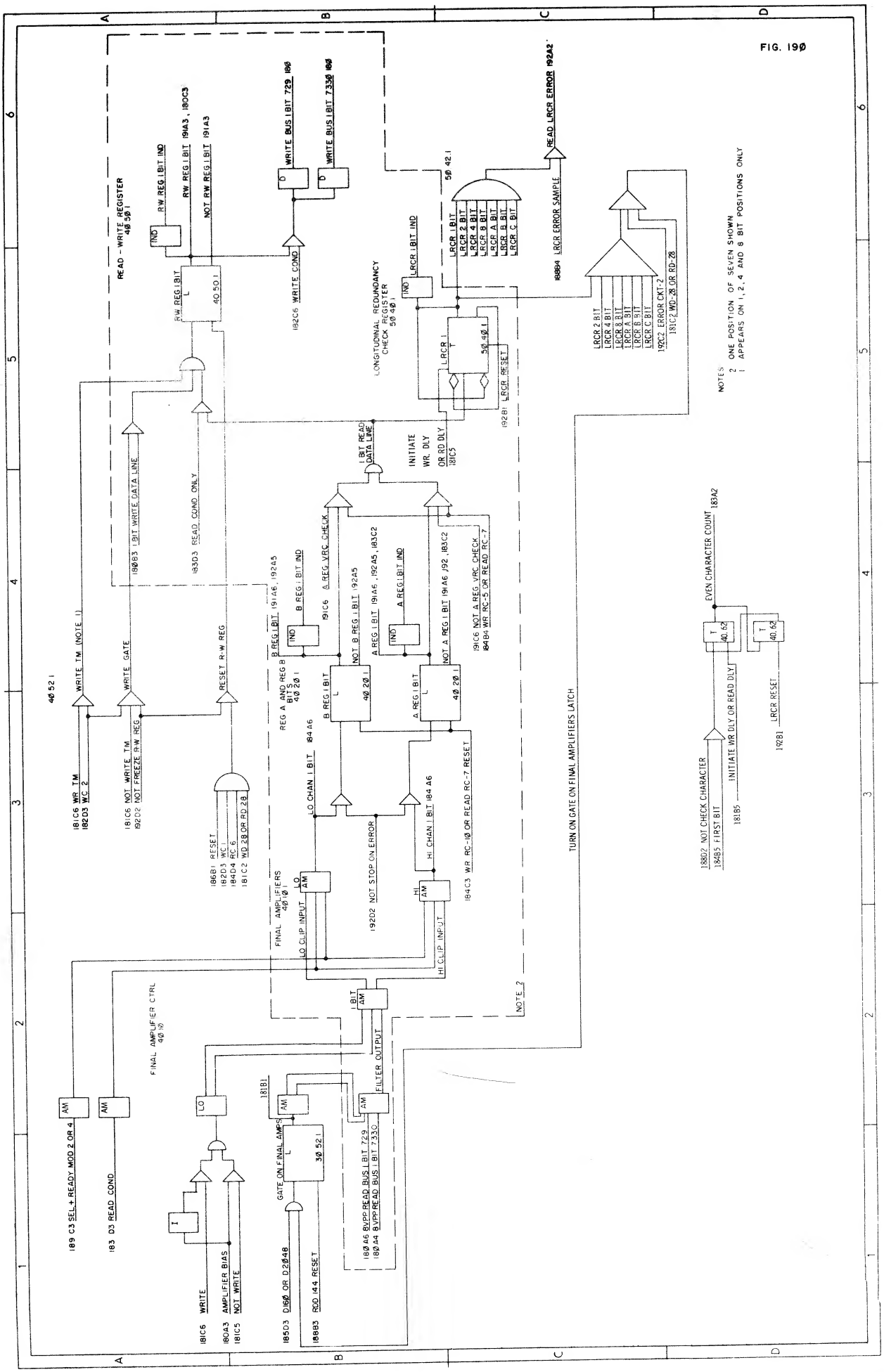


Figure 190. Final Amplifiers

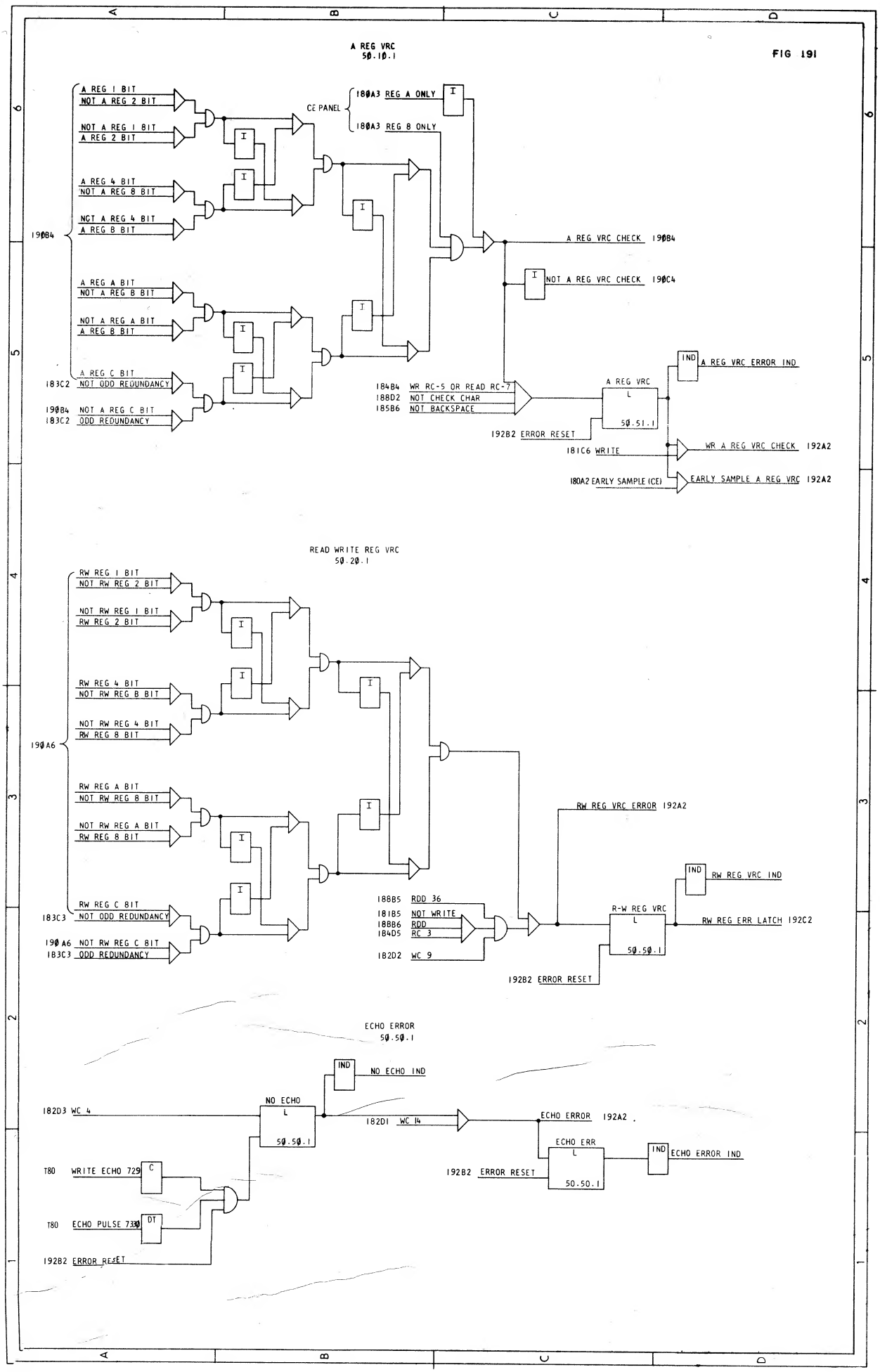


Figure 191. Error Circuits I

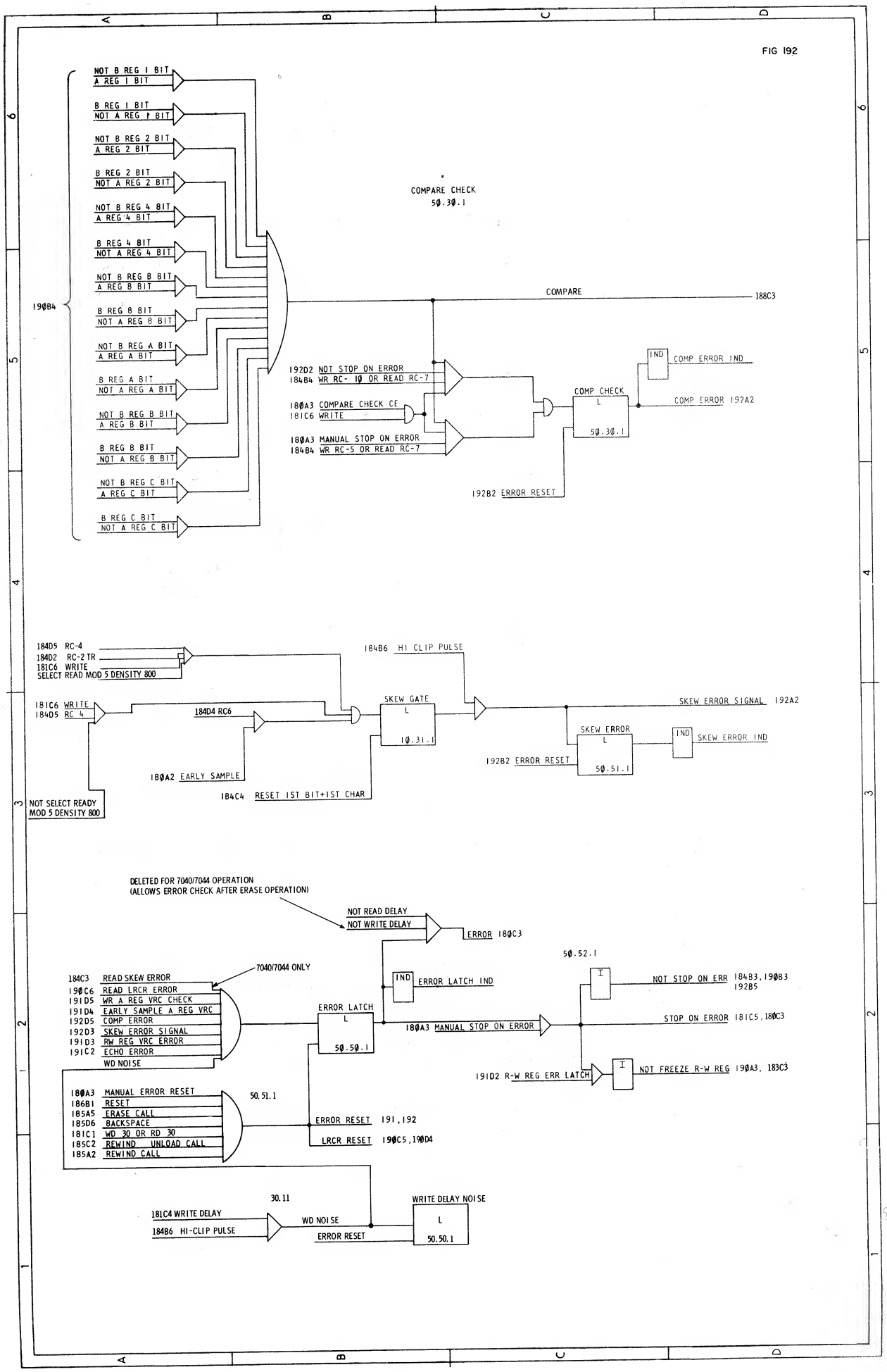


Figure 192. Error Circuits II

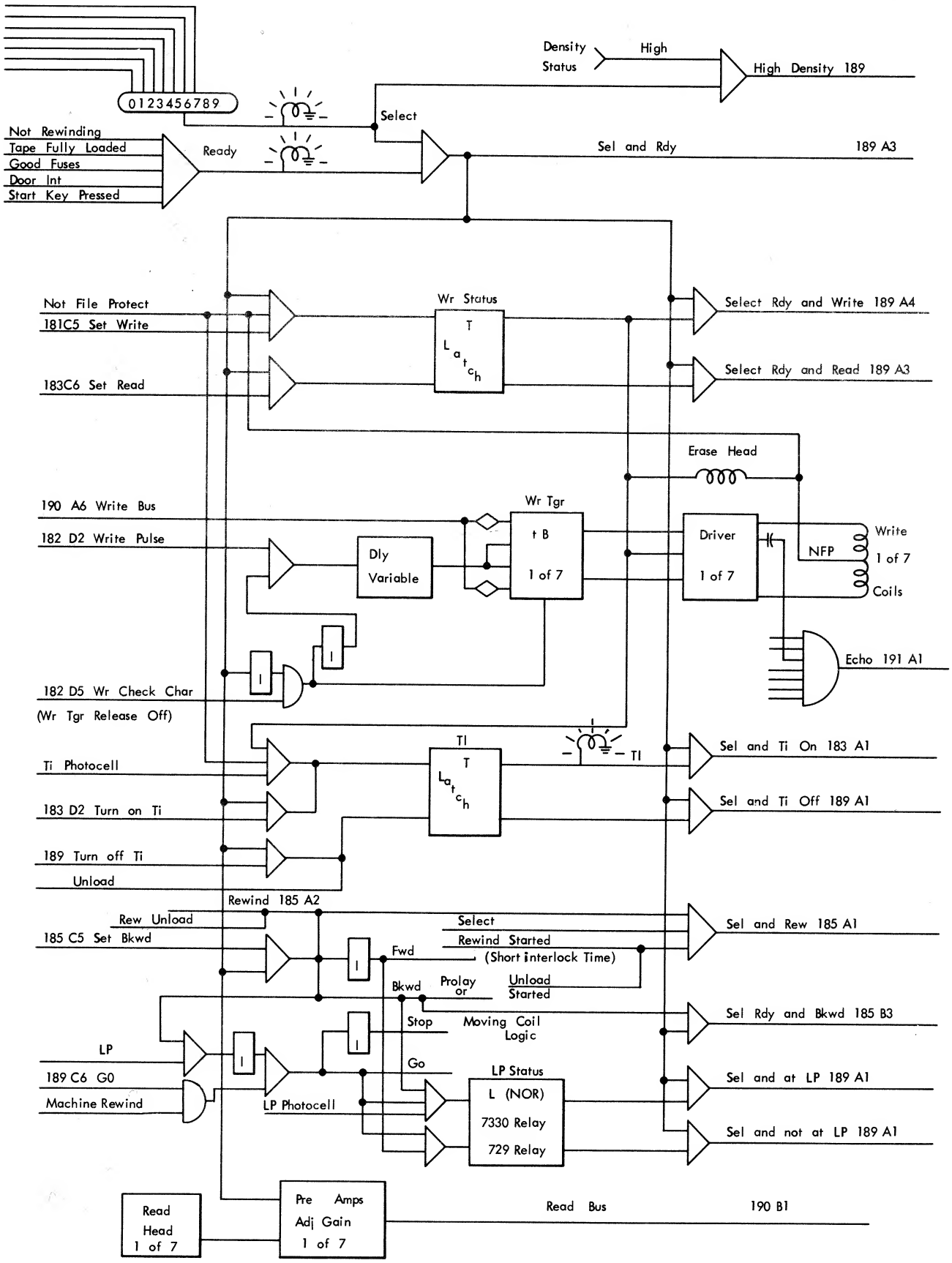


Figure T 80. Tape Unit Response Logic

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